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MODEL 8155
SYNCHRONIZED TIME CODE
GENERATOR

SERIAL NO. 185

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SYSTRON DONNER

INSTRUCTION MANUAL

MODEL 8155
SYNCHRONIZED TIME CODE
GENERATOR

SERIAL NO. 185

(D)

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SYSTRON DONNER CORPORATION

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SYSTRON DONNER
CORPORATION

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Please specify both model and serial number in all correspondence concerning Systron-Donner instruments. Address all inquiries on operation or applications to your nearest sales representative; or, Sales Manager, Data Products Division, Systron-Donner Corporation, 935 Detroit Avenue, Concord, California 94518

Whenever a Systron-Donner instrument requires service, the nearest Systron-Donner representative should be contacted; all representatives will provide immediate service or arrange factory returns when necessary.

STANDARD OPTIONS

Standard options installed in your unit are checked below. Circuit descriptions for these options are provided in Chapter 6. Special modifications, when included, are described in Chapter 7.

SERIAL NUMBER 185

OPTION	DESCRIPTION
☐ A12A	Slow Code, Type A
☐ A12B	Slow Code, Type B
☐ A16	Control Bit Insertion
☐ A16C	Control Bit Translation
☐ A16D	Control Bit Translation and LED Display
☐ A19	Group Parallel BCD Outputs
☐ A21	Computer Read Command
☐ B11	Crystal Oscillator with stability (± 4 parts in 10^9)
☐ B13	Crystal Oscillator with stability (± 4 parts in 10^9)
☐ B14	Crystal Oscillator, Zero Warmup (± 5 parts in 10^7)
☐ C11	IRIG A (10 kHz) Code
☑ C11Q , C12Q	IRIG A (10 kHz) Output Code
☐ C12A	Binary Seconds (17 Bits in Code)
☐ C12B	Binary Seconds (TOD) Parallel Output
☐ C17	NASA 28-Bit (100 Hz) Code
☐ C17Q	NASA 28-Bit (100 Hz) Output Code
☐ C18	NASA 36-Bit (1 kHz) Code
☐ C18Q	NASA 36-Bit (1 kHz) Output Code
☐ C26	XR3 (250 Hz) Code
☐ C26A	XR3 (1 kHz) Code
☐ C26P	XR3 (1 kHz) Output Code
☐ C26Q	XR3 (250 Hz) Output Code
☐ C31	IRIG G (100 kHz) Code
☐ C31Q	IRIG G (100 kHz) Output Code
☑ C41	IRIG A,B Switch Selectable

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OPTION	DESCRIPTION
☐ C47	XR3 (250 Hz/1 kHz) Switch Selectable
☐ C48	IRIG H (100 Hz)
☐ C48A	IRIG H (1 kHz)
☐ C48P	IRIG H (1 kHz) Output Code
☐ C48Q	IRIG H (100 Hz) Output Code
☐ C49	WWV Code
☐ C50	WWVB Code
☐ D12	Buffers, Positive Level
☐ D13	Buffers, Negative Level
☐ D14	Buffer Storage
☐ E14	Parallel BCD Output, Milliseconds
☑ E20	Days
☐ E22	Generate Preset and Control
☐ E22A	Generate Preset and Control (Option E20)
☐ L12	48 Hz to 440 Hz Operation
☐ L13	AC/DC Power Supply
☐ P20	Remote Slow Code Rate Select
☐ S11	External Synchronization
☐ S11A	WWV Synchronization
☐ S12	Propagation Delay Control
☐ S13	Analog Filters
☐ S14	Analog Filters with Remote Select
	Special Modifications (See Chapter 7)

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CHAPTER 1
GENERAL DESCRIPTION

1.1 INTRODUCTION

The Model 8155 Synchronized Time Code Generator is a time code generator which is usually operated in synchronism with an input reference time code. A reader section decodes the incoming reference time and uses this information to synchronize the generator section.

The generator can be equipped to output up to five serial time codes with a variety of optional formats all synchronized with the input reference code. Both modulated and demodulated outputs can be provided. Time information is displayed and supplied as buffered, parallel BCD output in hours, minutes and seconds. Days are optional.

The basic unit is designed to accept the IRIG B time code as the reference input. (Other time code formats may be substituted on an optional basis.)

During normal (synchronized) operation, a front panel Sync lamp is on. Internal error bypass and other logic circuits incorporating digital filtering, compensate for minor dropouts and brief noise in the input code structure. In effect, these minor defects are ignored and the unit is maintained in synchronism.

During abnormal conditions in which there are bit errors or loss of input, the Sync lamp is turned off and the Model 8155 continues operating using its internal time base for control. Upon restoration of the input code and after three consistant, good time code frames, the Model 8155 automatically resynchronizes the generator with the input reference code and the Sync lamp is turned back on.

A front panel mounted meter monitors the level of the input signal. The meter is usually set to midscale for a nominal input signal level.

The Model 8155 may be operated as a "stand-alone" generator after it is synchronized with the reference, simply by removing the input. A generator preset option adds preset and mode controls to the basic unit which permit the manual entry of initial time and operation of the generator in hold or stop. Many other standard options are also available.

The Model 8155 is constructed with silicon semiconductors and monolithic IC's assembled on printed-circuit, plug-in modules for reliability and ease of maintenance.

1.2 SPECIFICATIONS

Specifications for the Model 8155 are listed in Table 1.1.

TABLE 1.1 SPECIFICATIONS

Inputs	
External Time Base:	A 1 MHz input at 1 V p-p (nominal) into 1 kΩ through rear panel mounted BNC. Selected by rear panel switch.
Input Code:	An IRIG B (single ended or balanced) modulated time code in the forward direction via rear panel mounted barrier strip. Carrier - 1 kHz (IRIG B) Amplitude - -30 dBm to +20 dBm Ratio - 2:1 to 6:1 Input Z - 600 Ω balanced
Outputs (All outputs are short-circuit-proof to ground)	
Parallel BCD Outputs:	24 parallel lines (20 active bits) representing time-of-day in hours, minutes and seconds through rear panel mounted 50-pin connector (mate supplied). The Days Option adds 12 bits (10 active) to the same connector. Code: 8-4-2-1 Logic: "1" = +5 (±0.5 V) behind 6 kΩ "0" = 0 (+0.5 V) 12 mA sink
Modulated Code Outputs: (Output Code Options)	Adjustable from 0 to 10 V p-p from low impedance 15 mA source. Ratio adjustable from 2:1 to 6:1. Connectors are rear panel mounted BNC. Code formats optional.
DC Level Shift Code Outputs: (Output Code Options)	Adjustable from 0 V to 10 V p-p into 600 Ω. Connectors are rear panel mounted BNC. Code format optional.
Internal Time Base:	Crystal controlled oscillator with an aging rate of 1 X 10^{-7}/ day and an overall stability of 1 X 10^{-5}/day over a temperature range from 0°C to +60°C.

TABLE 1.1 SPECIFICATIONS (Cont'd)

Internal Time Base: (Cont'd)	Provision is included for an external 1 MHz input (see above). Options with higher stability may be substituted.
Display:	A 6-digit in-line, in-plane display indicates time-of-day in hours, minutes and seconds. Days Option adds 3 digits. Numeral height is 0.55" (14 mm).
Synchronization:	All outputs (parallel and serial) are synchronized to within ±10 µsec with reference to the "On Time" mark of the input reference code.
Time Set: (Optional)	A 6 or 9-digit thumbwheel switch register for selecting the initial starting time. Option also adds a Mode switch.
Environment:	Operating - 0°C to 50°C at up to 95% relative humidity. Storage - -55°C to +85°C
Power:	115/230 V ±10%, 48-62 Hz at less than 65 watts.
Package:	3-1/2" (8.9 cm) high by 19" (48.3 cm) wide by 17" (43.1 cm) deep. Removable rack flanges. Chassis drilled for Jonathon 120 QD series slides. Weight approximately 25 lbs (11 kg) net, 35 lbs (16 kg) shipping.

CHAPTER 2
INSTALLATION

2.1 INITIAL INSPECTION

As soon as the instrument is received, verify that it is intact and as ordered. Inspect it for damage. If any shipping damage is found refer to the warranty at the front of this manual and to subsection 2.2 for repackaging and shipping instructions.

As soon as possible, the instrument should be installed and given a thorough electrical inspection. Should the instrument fail to operate properly or fail to meet the listed specifications, immediately contact your Systron-Donner representative.

2.2 STORAGE AND RESHIPMENT

Environmental conditions during storage and shipment should be limited as follows:

Maximum Temperature: 185°F (85°C).

Minimum Temperature: -69°F (-55°C).

To protect your instrument during shipment or storage, use the best packaging methods available. Your Systron-Donner field office can provide materials similar to those used for original factory packaging. Contract packaging companies can provide dependable packaging on short notice.

General packaging instructions:

1) Wrap the instrument in heavy paper or plastic before placing it in the shipping container.
2) If possible, use the original container designed for the instrument. Otherwise, use a strong carton (350 lb.sq.in. bursting strength) or wooden box to house the instrument.
3) Use plenty of packaging material around all sides of the instrument and protect the front panel with cardboard strips.
4) Seal the package with strong tape or metal bands. Mark the package with "DELICATE INSTRUMENT".
5) Refer to the warranty at the front of this manual and check with your Systron-Donner field office for shipping instructions. All correspondence should refer to the instrument by its model number and full serial number.

2.3 POWER REQUIREMENTS

The Model 8155 can operate from 115 V or 230 V ±10%, 48 to 62 Hz. The unit is normally shipped equipped for 115 V operations. To adapt

it for 230 V operation push the rear panel selector switch, S101, to the "230" position and change Fuse F1 from 2A Slo-Blo to 1A Slo-Blo.

The Model 8155 is equipped with a standard three conductor power cord that automatically grounds the instrument when a matching power receptacle is available. An adapter which provides an instrument ground should be used whenever the power cord must be connected to a two-contact outlet.

2.4 INITIAL TURN-ON AND ADJUSTMENT

Initial turn-on should be accomplished as soon as possible after receipt of the instrument as part of the initial electrical inspection. This procedure checks the Model 8155 for any internal shipping damage.

1) Connect the unit to an appropriate ac power source after first checking that the rear panel power voltage selecter switch is in the correct position. Turn the front panel power switch ON.

2) Check that the rear panel 1 MHz EXT-INT switch is in the INT position. This selects the internal time base oscillator.

3) Connect the input reference time code to the rear panel INPUT CODE connector. The front panel INPUT LEVEL meter may be set to midscale by adjusting the meter set potentiometer located behind the meter inside the instrument.

4) Check the Modulated Code output(s). These have been factory set to approximately 3 volts p-p at the output. The output(s) may be observed at the rear panel BNC or at the "MOD" test point on the associated modulator card. The amplitude may be adjusted on the same card. The same is true of the modulation ratio which is factory set at 3:1. The ratio control is labeled "RATIO" on the modulator card.

5) Check the Level Shift output(s). These may be adjusted by manipulating the "DC" control on the associated modulator card.

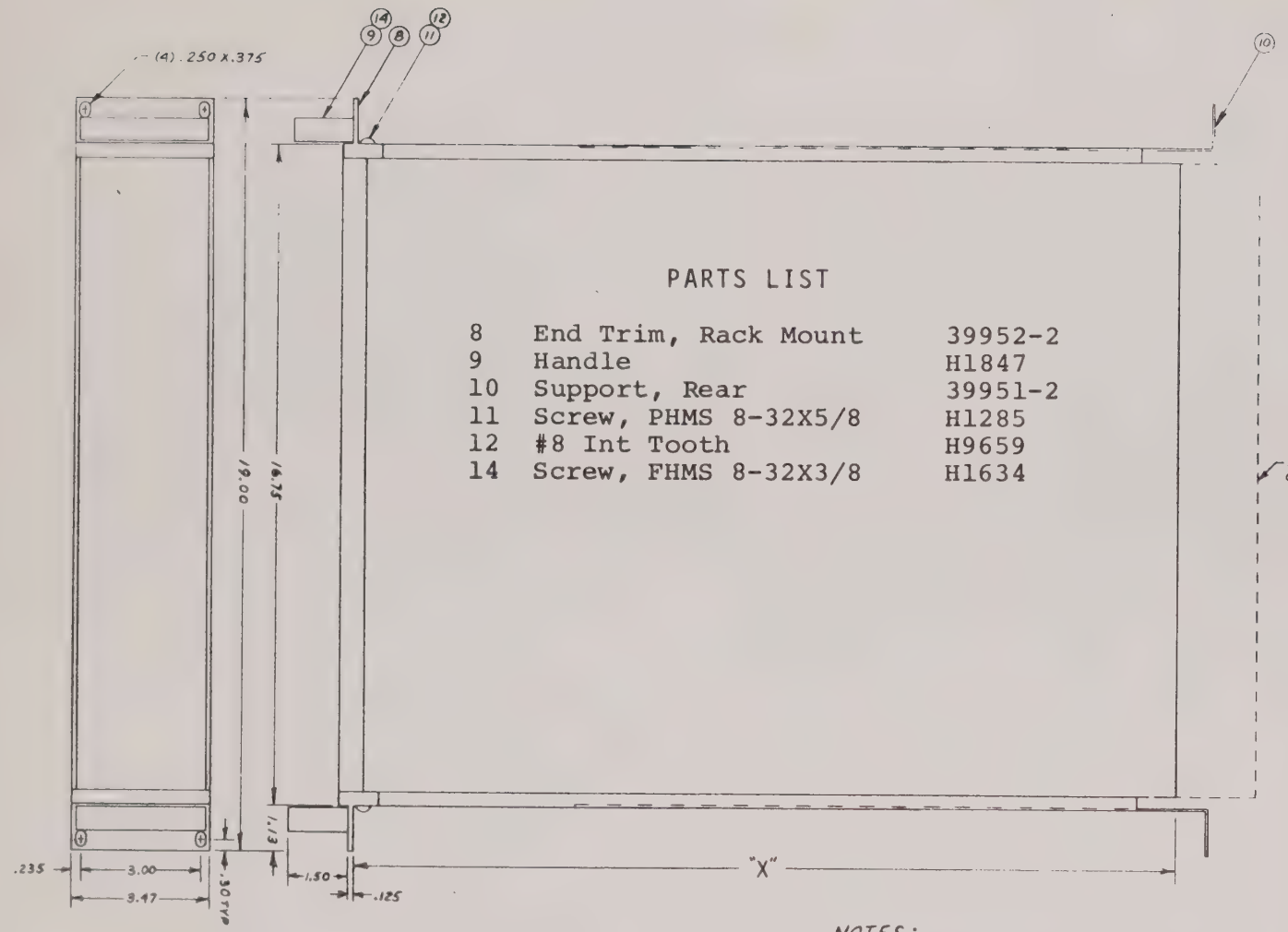
2.5 INSTALLATION

The Model 8155 is normally supplied with hardware for rack-mount installation as shown in Figure 2.1.

For convenience, the unit has been drilled for 20" Jonathan 120 QD series slides. When slides are used the rear support brackets (Item 10) are removed.

NOTE

Under no condition should air flow through the outlet hole in the rear of the unit be obstructed.



TABULATION		
P/L #	"X"	MSTR. DEPTH
39986-1	8.75	9.12
39986-2	10.75	11.12
39986-3	12.75	13.12
39986-4	14.75	15.12
39986-5	16.75	17.12
39986-6	18.75	19.12
39986-7	20.75	21.12

NOTES:
1. INSTR. ARE DRILLED TO ACCEPT 20" JONATHAN 120 QD SERIES SLIDES
2. ITEM 10 DELETED WHEN SHIPPED W/SLIDES

FIGURE 2.1 3 1/2" FULL RACK ASSEMBLY #039968-4-5 REV A

CHAPTER 3
OPERATION

3.1 GENERAL

The Model 8155 is ready to operate immediately after turning on the power. With the exception of the Input Level Meter adjustment, preliminary adjustments and calibration are not normally required.

3.2 FRONT PANEL CONTROLS AND INDICATORS

Table 3.1 lists the Front Panel controls and indicators.

TABLE 3.1 FRONT PANEL CONTROLS AND INDICATORS

Index	Name and Type	Function
1	POWER ON/OFF: (Rotary Switch, S1)	Applies ac power to instrument.
2	SYNC Indicator: (Amber Lamp)	Lamp is on when unit is synchronized with an input reference code.
3	Readout Indicators: (Polarized Window)	6-digit, in-line planar readout indicates time in hours, minutes and seconds. Days Option adds 3-digits.

3.3 REAR PANEL INPUTS AND OUTPUTS

Table 3.2 lists the Rear Panel inputs and outputs.

TABLE 3.2 REAR PANEL OUTPUTS AND INPUTS

Index	Name and Type	Function
1	J1 BCD OUTPUT (50-pin connector)	BCD outputs of front panel display readings.
2	600 Ω CT SHLD: (Barrier Strip)	600 Ω balanced input for the reference code.
3	J17 EXT 1 MHz: (BNC Connector)	External 1 MHz Time Base Input.
4	INT 1 MHz EXT: (Slide Switch S14)	Selects INT or EXT 1 MHz Time Base.

TABLE 3.2 REAR PANEL OUTPUTS AND INPUTS (Cont'd)

Index	Name and Type	Function
5	115/230 ±10%: (Receptical, Power Cord, J101)	Connects to main power line (115/230 V, 48 to 62 Hz).
6	115/230: (Slide Switch, S101)	Adapts unit for 115 or 230 V power.
7	F1 SLO-BLO: (Fuse Holder)	Main power fuse (2 A-115 V/ 1 A-230 V).

CHAPTER 4
MAINTENANCE AND CALIBRATION

4.1 FACTORY SERVICE

When the instrument requires service, the nearest Systron-Donner representative should be contacted. He can provide field service or arrange for factory returns, when necessary. Address all inquiries on operation or applications to your nearest sales representative; or, **Sales Manager:**

SYSTRON-DONNER CORPORATION
DATA PRODUCTS DIVISION
935 Detroit Avenue
Concord, California 94518
Phone: (415) 798-9900
TWX: 910-481-5780
Cable: SYSTRONDONNER

Specify both model and complete serial number in all correspondence.

4.2 ROUTINE MAINTENANCE

A regular program for maintenance and inspection every five to six months is recommended for this unit. As part of these regular procedures, the instrument should be checked in the following manner:

1) Disconnect ac power and remove the top and bottom covers.

2) Make a thorough visual inspection of all wiring and cables. Check for frayed, loose, or burned wires.

3) Check the physical integrity of all components. Look for burned or cracked components, loose solder connections, leakage of insulation compounds, and general physical damage. When a printed circuit board contains integrated circuit packages, ensure that all packages are firmly mounted. Never unnecessarily remove and replace a package.

4) Check all front panel switches and controls for loose or broken terminals, loose or sticking shafts, etc.

5) If the internal panel surfaces and components have an excessive amount of dust deposited on them, use a soft brush and low pressure stream of air to remove the foreign material.

CAUTION

Do not clean P.C. boards or small internal components with a stiff brush or solvents, since damage to the circuits may result. A high-powered vacuum cleaner device should not be used on small internal components.

6) Wipe the external surfaces of the instrument with a soft damp cloth to remove dirt, fingerprints, and other foreign materials.

7) Replace the top and bottom covers and reconnect ac power. Perform the Operational Test and Calibration Procedure Section 4.4). If performance does not match or exceed the specifications listed in Chapter 1 of this manual, corrective maintenance is in order.

4.3 PRINTED-CIRCUIT BOARD REPAIR

When replacing integrated circuits or other electronic components soldered to printed-circuit boards, the procedures indicated below must be followed or damage to the board may result:

1) Determine by troubleshooting techniques, which integrated circuit or discrete component(s) has failed.

2) Remove the defective component(s) from the board by cutting the pins or leads with a small diagonal clipping tool. (Always remove and replace the entire component.)

3) Apply heat (40-50 W soldering iron) sparingly to each of the cut pins or leads and remove from the board; clean the hole(s) with a toothpick or solder suction tool.

4) Form the tinned leads of the replacement part and insert in the printed circuit holes; solder, then trim leads to extend 1/16-inch beyond the back surface of the board. (Use only 63-37 solder with maximum 1/16-inch diameter.)

CAUTION

Always trim semiconductor leads only after soldered installation is complete. This procedure greatly lessens the possibility of component failure due to shock-wave damage caused by the trimming tool.

5) When soldering semiconductor devices and all small components, be sure to use a heat sink tool or long-nosed plier connected to the component lead(s) while each is being soldered. Allow the soldered connection to cool before removing the heat sink.

6) Clean all dirt and solder-flux from the printed-circuit traces by liberal application of isopropyl alcohol or freon-type solvents.

4.4 OPERATIONAL TEST AND CALIBRATION PROCEDURE

In the event of an equipment malfunction the following circuit description and adjustment procedure, if followed in the listed sequence, will allow the service engineer to isolate the trouble to a particular circuit card or subsection.

When the trouble is isolated the functional description and card information in Chapters 5 and 6, will facilitate repair.

WARNING

Dangerous high voltages are present in the power supply of this equipment. Use caution at all times when the protective covers are removed.

4.4.1 Recommended Test Equipment

The following test equipment or equivalent is recommended for use in servicing the Model 8155.

TABLE 4.1 TEST EQUIPMENT FOR MODEL 8155

Model	Manufacturer	
422	Tektronix, Inc.	Oscilloscope, 15 MHz bandwidth, triggered sweeps from 0.1 microseconds/cm to 5 sec/cm. Vertical sensitivity from .05 volts/cm to 20 volts/volts/cm.
6012	Tektronix, Inc.	Probe, 10:1 attenuation ratio, 17 pF capacitance.
7004A	Systron-Donner Corp.	DMM 10 MΩ input impedance, ±0.1% accuracy.
200AB	Hewlett-Packard Co.	Audio Oscillator, 20 Hz to 40 kHz coverage.
6250	Systron-Donner Corp.	Frequency Counter, 0 Hz to 50 MHz, 3 parts/10^{-7} per week.

In addition to the equipment listed above, a suitable source of time code input signals with known characteristics is required.

4.4.2 Power Supply Calibration Procedure (Dwg. #041810-7-9)

Check that fuse F1 is the proper size for the input voltage selected:

2A, 115 V

1A, 230 V

With an input of 115 V ac (230 V if so equipped) ±5%, 50/60 Hz. Check the following at the Power Supply P.C. Board, edge connector, P103.

1) +210 V ±25% at pins V, 18 (GND 20, X)
2) +21 V ±20% at pins S, 15 (GND BLACK TEST POINT)
3) +9 V ±20% at pins Y, 21 (GND BLACK TEST POINT)
4) -9 V ±20% at pin 2 (GND BLACK TEST POINT)
5) -21 V ±20% at pin 4 (GND BLACK TEST POINT)

Measure the +15 V supply on the BLUE (GND BLACK) Test Point and adjust R5 (15 V ADJ) for +15 V ±0.3 V.

Measure the -15 V supply on the VIOLET Test Point and verify that it is within ±0.3 V of -15 V. Readjust R5 is necessary so that both +15 and -15 V supplies are within ±0.3 V.

Measure the +5 V supply on the RED Test Point and adjust R19 (5 V ADJ) for 5 V ±0.1 V.

Measure the -5 V supply on the GREEN Test Point and verify that it is within ±0.1 V of -5 V. Readjust R19 if necessary so that both +5 and -5 V supplies are within ±0.1 V.

4.4.3 Oscillator Adjustment

The accuracy of the oscillator may be determined, relative to a frequency standard, by observing the rate of drift of an oscilloscope pattern as shown in Figure 4.1, Oscillator Accuracy Test.

If the pattern moves to the right, the frequency of the oscillator under test is lower than that of the frequency standard; if the pattern moves to the left, the frequency under test is too high.

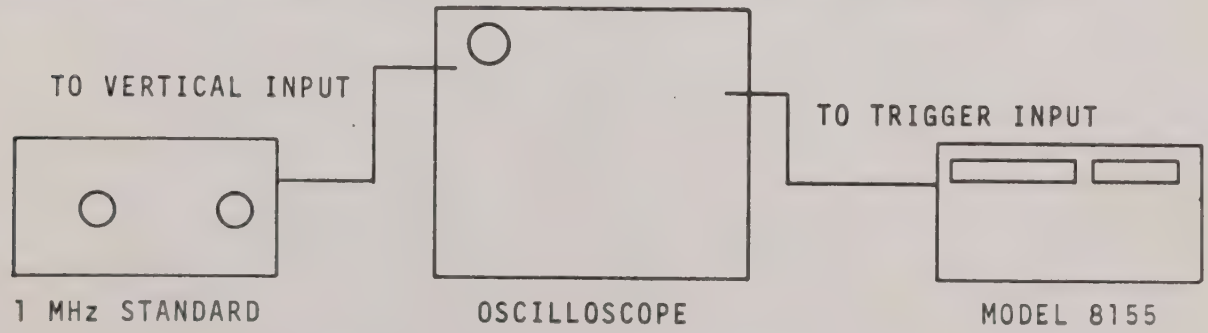


FIGURE 4.1 OSCILLATOR ACCURACY TEST

To check oscillator frequency (not stability):

1) Trigger the oscilloscope externally with the 1 MHz internal oscillator of the Model 8155 (available at pin 13, A27).
2) Connect a 1 MHz frequency from an external standard to the vertical input of the oscilloscope.
3) Set the oscilloscope sweep time to 0.1 s/cm and adjust the controls to obtain a presentation of a 5 V p-p wave form.
4) Horizontal drift of the oscilloscope displayed in cm/s is the difference from the standard frequency in parts/10 . If necessary, adjust the oscillator (C3 on the Time Base Card) until drift is negligible.

TABLE 4.2 OSCILLATOR ACCURACY

Drift	Accuracy
1 cm/0.1 sec	1 part in 10^6 (10 Hz)
1 cm/sec	1 part in 10^7 (1.0 Hz)
1 cm/10 sec	1 part in 10^8 (0.1 Hz)

4.4.4 AGC & Cycle Detector Adjustment (Dwg. #021569-7-9)

Preliminary Set-Up

Connect Time Code Source to "Code In" BNC on rear panel of instrument. Adjust the input to approximately 3 V p-p.

CAUTION

Do not place AGC & Cycle Detector on extender board when performing these adjustments.

AGC Level Adjustment

Monitor "TRIG" Test Point with oscilloscope.

1) Adjust R4 "AGC" potentiometer so that the large cycles (see Figure 4.2, ACG Level Adjustment) are 2.75 V p-p 5%.
2) Reduce level of incoming code to approximately 1 V p-p.
3) Allow approximately 5 seconds for AGC to recover. Signal at "TRIG" Test Point should remain the same amplitude as adjusted in Step 1).

Cycle Detector Adjustment

Monitor "TRIG" Test Point with oscilloscope.

1) EC (Each Cycle) adjustment.

   Set oscilloscope to trigger positive (+), external trigger.

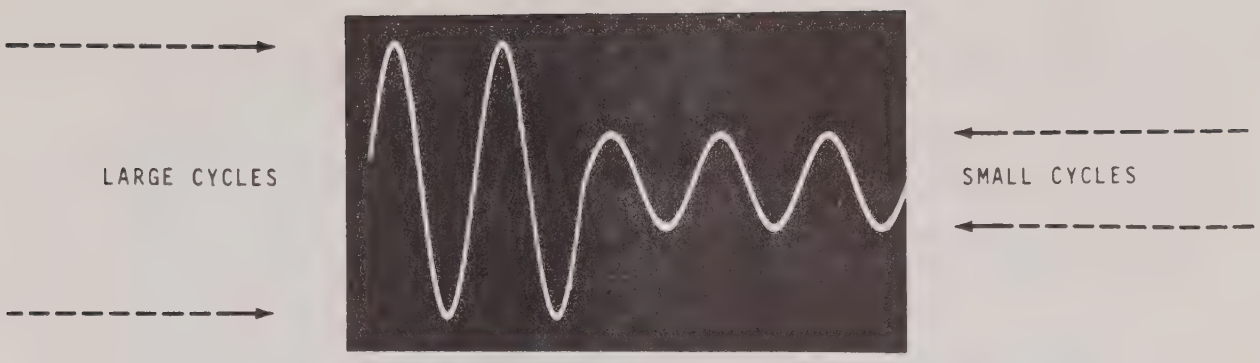


FIGURE 4.2 AGC LEVEL ADJUSTMENT

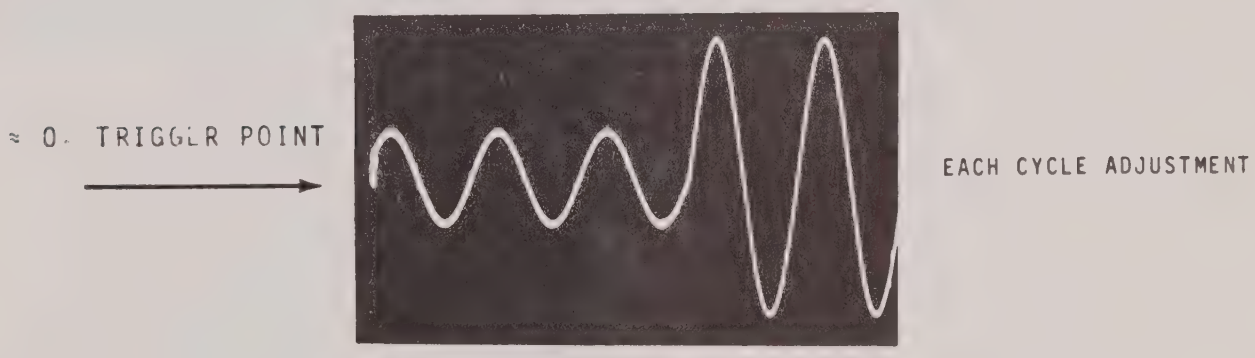


FIGURE 4.3 CYCLE DETECTOR ADJUSTMENT

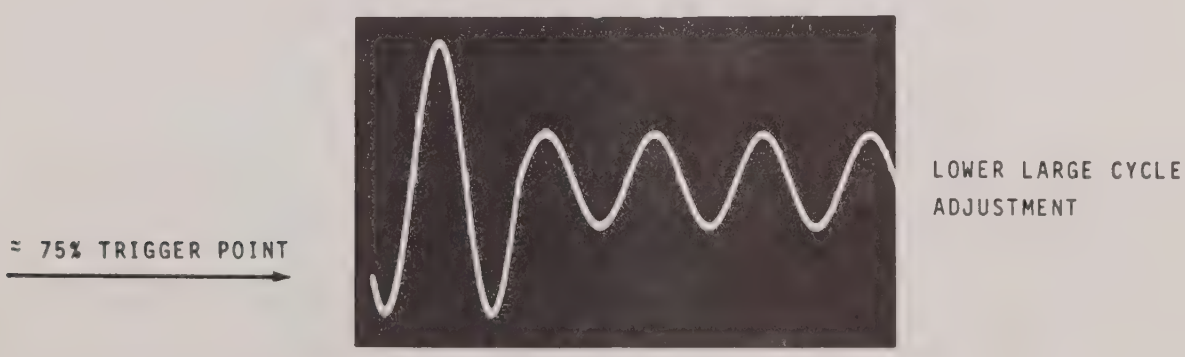


FIGURE 4.4 LOWER LARGE CYCLE ADJUSTMENT

Connect external trigger input of oscilloscope to "EC" Test Point.

Turn R25 "EC" Adjust, full clockwise. Turn in the CCW direction until each cycle is triggering approximately at the cros crossover of the small cycles (see Figure 4.3, Cycle Detector Adjustment).

2) $\overline{\text{LLC}}$ (Lower Large Cycles) adjustment:

Set oscilloscope to trigger negative (-), external trigger. Connect external trigger input of oscilloscope to $\overline{\text{LLC}}$ Test Point.

Turn R34 "LLC" Adjust, full clockwise. Turn in the CCW direction until the lower large cycles are triggering approximately 75% of the way down on the negative slope of the lower large cycles (see Figure 4.4, Lower Large Cycle Adjustment).

4.4.5 Input Level Meter Adjustment

The "Meter Adj." potentiometer R1, is located on a bracket directly behind the Input Level meter. Adjust for a midscale meter reading with the input reference code amplitude at the nominal operating level expected during normal service.

CHAPTER 5
FUNCTIONAL DESCRIPTION

5.1 GENERAL

The basic Model 8155 consists of a time code generator section which can operate independently or in synchronism with an input reference code fed through a time code reader section.

The basic generator accumulates, displays and outputs (parallel BCD) Time-of-Day in hours, minutes and seconds. The addition of three digits of days is optional. The same is true of the up to five simultaneous serial output codes which can be accommodated.

The basic reader accepts the IRIG B modulated time code on a 1 kHz carrier. Other codes may be substituted as options.

Standard options, when included, are described in Chapter 6. Special modifications, if any, are described in Chapter 7. The basic unit is described below, first as an independent time code generator and second as a synchronized reader-generator.

5.1.1 Reference Designations

Reference designations are confined to the assembly being discussed since it is usually clear from the context which assembly is involved.

When citing a sub-element of a multielement integrated circuit, the reference designation of the IC is given followed by the number of the output terminal.

When citing flip-flops formed from two gates on the same chip the reference designation of the chip is given followed by the two output pins.

The reference designations used in the Model 8155 are listed in Table 5.1.

TABLE 5.1
REFERENCE DESIGNATIONS

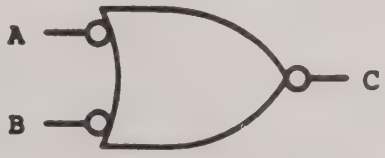
A or U	Integrated Circuit
C	Capacitor
CR	Diode
DS	Lamp
F	Fuse
FL or Z	Filter
J	Jack
L	Inductor
P	Plug
Q	Transistor
R	Resistor
S	Switch
T	Transformer
TP	Test Point
W	Jumper
X	Socket

5.1.2 Logic Functions

The Logic symbols and functions used in the Model 8155 are described as follows: Truth tables and detailed explanations are given where necessary in order to assist qualified maintenance personnel in the repair and upkeep of the instrument.

AND Gate

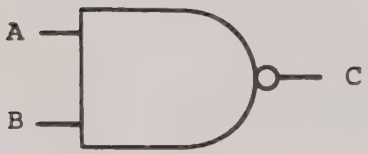
INVERTED NOR Gate



A	B	C
0	0	0
0	1	0
1	0	0
1	1	1

The AND Gate and **INVERTED NOR Gate have the same** truth table.

NAND Gate

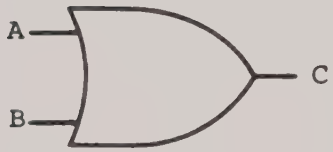


INVERTED OR Gate

A	B	C
0	0	1
0	1	1
1	0	1
1	1	0

The NAND Gate and INVERTED OR Gate have the same truth table.

OR Gate

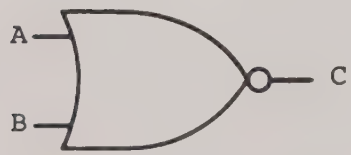


INVERTED NAND Gate

A	B	C
0	0	0
0	1	1
1	0	1
1	1	1

The OR Gate and INVERTED NAND Gate have the same truth table.

NOR Gate

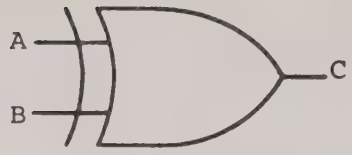


INVERTED AND Gate

A	B	C
0	0	1
0	1	0
1	0	0
1	1	0

The NOR Gate and INVERTED AND Gate have the same truth table.

EXCLUSIVE OR

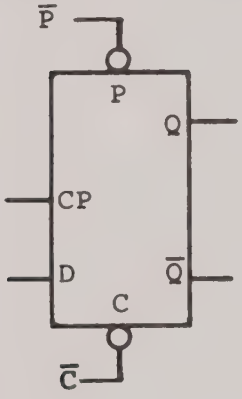


A	B	C
0	0	0
0	1	1
1	0	1
1	1	0

EXCLUSIVE NOR

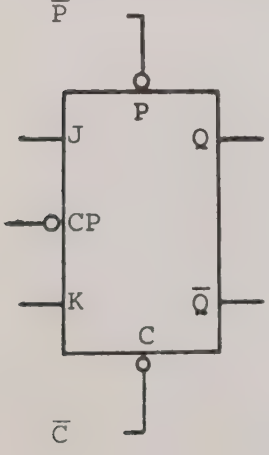
A	B	C
0	0	1
0	1	0
1	0	0
1	1	1

D-TYPE Flip-Flop



1) Q assumes the state of the D input on the positive transition of the clock (CP) input.
2) The D input is locked out when the clock input is positive.
3) P and C override all other inputs.
4) If $\overline{P}$ and $\overline{C}$ are both at Logic 0, the Q and $\overline{Q}$ outputs are both at Logic 1.
5) At a set condition, Q is Logic 1. At a clear condition, Q is a Logic 0.

JK-TYPE Flip-Flop



1) When J and K are both at a Logic 0, no change will occur.
2) When K is a Logic 1, Q will be a Logic 0.
3) When J is a Logic 1, Q will be a Logic 1.
4) When J and K are both at a Logic 1, the flip-flop will change state.
5) $\overline{P}$ and $\overline{C}$ override all other inputs.
6) CP is the clock input.

In some configurations it is possible to perform the AND and OR function simply by tying the outputs of certain gates together.

These functions are called DOT AND and DOT OR functions. The nature of the signals fed to the "DOT" determines whether the function is AND or OR. When several "DOTS" are present on a single line, the AND or OR symbol is used only once.

DOT AND

DOT OR

Logic 0 or Logic 1 denotes internal equipment logic levels. Logic "0" or Logic "1" denotes the logic levels of received or supplied data. Logic signals, when referred to in the text have the first letter capitalized. Equipment controls, when referred to in the text are capitalized.

5.2 GENERATOR OPERATION

The basic generator consists of; 1) A precision time base; 2) A minor counter; 3) A time-of-day (TOD) accumulator; 4) Parallel BCD output buffers (TOD), and 5) A TOD display. Each of these sub-sections is described briefly below. Detailed card descriptions, schematics and parts lists are provided at the end of this chapter. (A standard Generator Preset Option adds mode and preset switches for manual entry of start time for independent generator operation. A Days Option adds a days accumulator complete with parallel output buffers and a days display. In addition, up to five optional serial output code generators with adjustable, buffered outputs may be included to complete the Timing Terminal Unit. These options, when included, are described in Chapter 6.)

5.2.1 Time Base

The Time Base consisting of a 1 MHz Internal Oscillator with Shaper, a Start/Stop flip-flop, an Elapsed Time Gate and a 3-decade Divider chain is contained on card A27. (Refer to Block Diagram.) It supplies the 1 kpps (8×10^{-4}) input to the Minor Counter (A20), symetrical (carrier) rates to the shaper circuits and Z-rate inputs to the optional Code Generator card(s). Provision is included for the substitution of an external 1 MHz input and for the introduction of a sync signal.

5.2.2 Minor Counter

The Minor Counter (A20) is a 3-decade, parallel presetable counter which divides the 1 kpps input from the Time Base down to the 1 pps

Update signal required by the TOD Accumulator (A15). In addition, it decodes and buffers three pulse rates (1 pps, 10 pps, and 100 pps) with 10% duty cycle and provides two sets of buffered, parallel BCD milliseconds outputs; one set for internal distribution and the other optionally available for external use. The parallel preset feature is used to synchronize the Minor Counter when operating in synchronism with a reference code. (See paragraph 5.3.)

5.2.3 TOD Accumulator

The Time-of-Day Accumulator (A15) accepts the $\overline{1\ pps}$ (8×10^{-1}) output from the Minor Counter and divides it into units and tens of seconds, minutes and hours. The decade and scale-of-six dividers which accomplish this can be parallel preset as well as provide buffered parallel BCD outputs. This feature permits the time stripped from the input reference code to be entered through storage registers on A16. The parallel BCD outputs are fed to the TOD Display, to output Buffers on A14 and to optional Code Generator Cards. The 1 ppd (20 H) output is available as an input to the optional Days Accumulator A8.

5.2.4 Buffer

Twenty noninverting Buffers are provided on card A14 to supply parallel BCD TOD outputs for external use.

5.2.5 TOD Display

A 6-digit front panel, in-line, in-plane display for the presentation of TOD information in hours, minutes and seconds. Space is available for the addition of an optional 3-digit Days Display. Colons are provided between seconds and minutes, minutes and hours and (if included) between hours and days.

5.3 SYNCHRONIZED OPERATION

The reader section is used to synchronize the time code generator with an input reference code. The basic reader accepts the IRIG B time code on a modulated carrier. (Other input codes may be accomodated on an optional basis. See Chapter 6.) It developes on-time frame pulses which are used to synchronize the Time Base and Minor Counter. It strips the time information from the input code, varifies its accuracy and uses it to preset the Accumulator. A meter is provided to continuously monitor the level of the input signal.

The basic reader section consists of; 1) an AGC and cycle detector, 2) reader logic circuitry, 3) a dropout detector, 4) a frame marker length detector, 5) a bit error detector and 6) an input level meter. Each of these groups of circuits is described briefly below. Detailed card descriptions, schematics and parts lists are provided at the end of this chapter.

5.3.1 AGC and Cycle Detector

The modulated input code is fed through isolation transformer T1 to an AGC circuit on A26. (A high impedance, single ended input is optionally available.) This circuit establishes a standard level signal from which two output signals are extracted by Cycle Detectors on the same card. The first of these is the Each Cycle (EC) signal which is a square wave at the input carrier rate. The second is the Lower Large Cycle ($\overline{\text{LLC}}$) signal, which is produced whenever large cycles appear in the code. The $\overline{\text{LLC}}$ pulses are narrower and fall between transitions of the EC signal. This characteristic is used by the reader logic. Both outputs are fed to the Input Logic (A21), Reader Logic (A18) and Control Logic (A19) cards.

5.3.2 Reader Logic

In the basic unit the Reader Logic Card A18 translates IRIG Codes. It accepts the EC and LLC signals from the AGC and Cycle Detector A26, identifies the markers and bits and loads the time information into a 9-bit shift register in 2-digit bytes. It develops output strobe signals which load the seconds, minutes and hours bytes into a storage register on the TOD Error Detector A16 and the days bytes into similar storage on Days Error Detector A7 when this option is included. (Tenths-of-seconds are loaded into a register on the Reader Logic Card when translating the IRIG A Code.) The Reader Logic Card also develops complimentary BCD outputs representing the frame Y-time. These signals are used by the Input Logic A21 and Control Logic A19.

5.3.3 Dropout Detector

The dropout detector circuitry performs two basic functions. First a circuit on Input Logic Card A21 detects the presence of an input signal and second, a circuit on Control Logic Card A19 detects the presence of modulation on the input signal. If either of these circuits is not satisfied all synchronization is blocked and the time code generator continues operating from the internal time base.

5.3.4 Frame Marker Length Detector

The frame marker at X9Y9 time must be precisely eight large cycles long (IRIG Codes) for the frame sync signals to the Time Base and Minor Counter to be "on time". A circuit on the Input Logic Card verifies this and enables the generation of the sync signals only when this criterion is met. The Reader Logic, which includes some digital filtering, continues to synchronize the Accumulator through the Error Detector circuits even when the sync signals are blanked.

5.3.5 Error Detector

The time data error detector is made up of circuits on Control Logic A19, TOD Error Detector A16 and Days Error Detector A7 if the days

option is included. The Error Detector cards accept the time data from the Reader Logic in bytes and stores it in a parallel storage register. (Tenths-of-seconds bits are stored on the Reader Logic Card when reading IRIG A.) The contents of this register are compared, in parallel, with the contents of a duplicate accumulator which is part of the Error Detector circuitry. This duplicate accumulator is updated at the start of each frame in synchronism with the main accumulator. This means that it will contain the same information just read into the storage register once the unit is synchronized.

Synchronism is achieved as follows: Time data from the Reader are loaded into the storage register and compared with the contents of the duplicate accumulator as mentioned above. For the first frame the result will be an error (COINcidence line low). This signal resets a "Good Frame" counter on the Control Logic Card and turns the Sync lamp off. Immediately after this, but before the end of the frame, the contents of the storage register are loaded into the duplicate accumulator.

When the next frame starts, the duplicate accumulator is updated. The next frame time data from the Reader are loaded into the storage register and compared with the new contents of the duplicate accumulator. If everything went well the result of this comparison will be good (COIN line high) and the Good Frame counter is advanced one count. However, the Sync lamp remains off and the main accumulator is not disturbed. At the start of the next frame the duplicate accumulator is again updated and the above events repeated. This procedure is continued until the Good Frame counter reaches its programmed count limit which may be 3,7 or 13 frames. (The normal limit is 3 frames.) When this occurs the counter locks up, the contents of the duplicate accumulator are loaded into the main accumulator and the Sync lamp is turned on. The Generator accumulator section is now synchronized with the time data output from the Reader section.

Now if at any time an error is detected due to loss of a bit in the input code or an equivalent malfunction, the Good Frame counter is reset and the above procedure repeated to regain synchronization. During this period the main accumulator continues to run undisturbed.

5.3.6 Input Level Meter

The Input Level Meter indicates the average level of the input reference code. It may be set to midscale for the chosen level within the specified input range. It provides a quick means for checking the input whenever synchronism is lost.

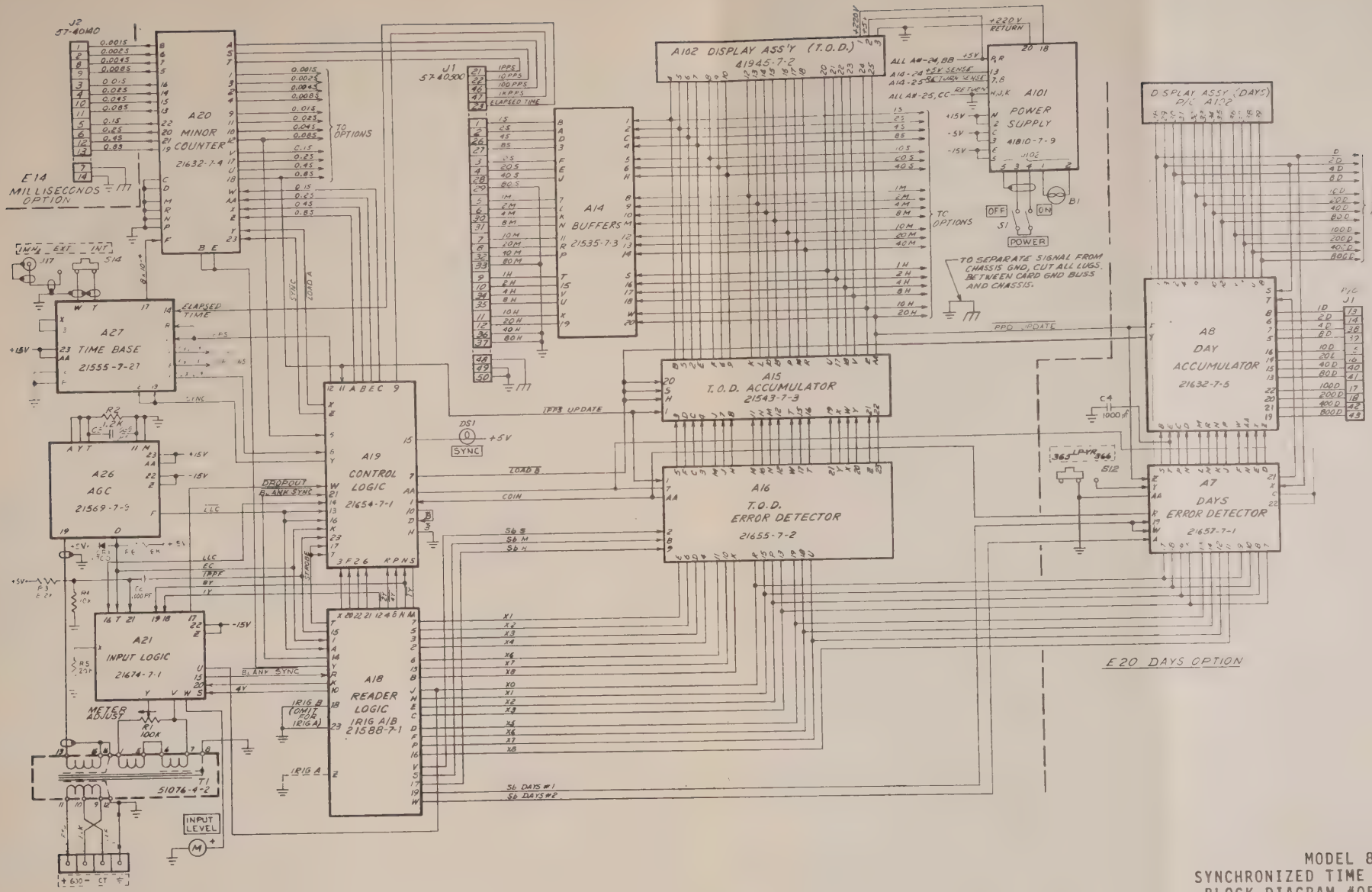
TABLE 5.2
CIRCUIT DESCRIPTION INDEX INFORMATION

Location	Description	Schematic #	Page #
A1-6	Reserved for Options		
A7	Days Error Detector (Option)	21657-7-1	--
A8	Days Accumulator (Option)	21632-7-5	--
A9-13	Reserved for Options		
A14	Buffer	21535-7-3	5-14
A15	Time-of-Day Accumulator	21543-7-3	5-18
A16	Time-of-Day Error Detector	21655-7-2	5-45
A17	Reserved for Options		
A18	IRIG Reader Logic	21588-7-1	5-31
A19	Control Logic	21654-7-1	5-41
A20	Minor Counter	21632-7-4	5-36
A21	Input Logic	21674-7-1	5-49
A22-25	Reserved for Options		
A26	AGC and Cycle Detector	21569-7-9	5-26
A27	Time Base	21555-7-27	5-22
A101	Power Supply	41810-7-9	5-54
A102	Display Assembly (TOD)	41945-7-2	5-61

All plug-in modules are designed so that each card will fit into position only if it is correctly aligned; however, caution must be exercised to ensure that a card is installed in the correct card slot. Latching handles on all cards are numbered to facilitate correct installation.

CAUTION

When mounting a card on the extender board, it is possible to install the card backwards which could result in serious damage.



MODEL 8155
SYNCHRONIZED TIME CODE GENERATOR
BLOCK DIAGRAM #051206-7-1 REV G

PARTS LIST

FINAL ASSEMBLY #051207-8-1

REF.	DESCRIPTION	SD PART NO.	QTY.
	SHIPPING ASSEMBLY #051207-4-1 (REV B)		
	Assembly, Test	051206-4-1	1
	Trim, Front Panel Top	041997-1-1	1
	Trim, Front Panel Bottom	033762	1
	Trim, Insert	05116211	1
	Trim, Rack Mount End	03995202	2
	Window	05100111	1
	Handle	100927	2
	Trim, Side	039859-5	4
	Bracket, Mounting Cover	039857	4
	Cord, Vinyl	100955	A/R
	Cover, Top	033760-5	1
	Cover, Bottom	033761-5	1
	Cord, Line (P101) Ship with	102407	1
	Connector, 50-contact	101157	1
	Support, Rear	039951-2	2
	TEST ASSEMBLY #051206-4-1 (REV D)		
	Assembly, Chassis	05120301	1
A14	Assembly, Buffer	021535-4-3	1
A15	Assembly, TOD Accumulator	021543-4-3	1
A16	Assembly, TOD Error Detector	021655-4-2	1
A18	Assembly, Reader Logic	021588-4-1	1
A19	Assembly, Control Logic	021654-4-1	1
A20	Assembly, Minor Counter	021632-4-4	1
A21	Assembly, Input Logic	021674-4-1	1
A22	Assembly, Extender	021507-4-1	1
A26	Assembly, AGC	021569-4-9	1
A27	Assembly, Time Base	021555-4-27	1
	CHASSIS ASSEMBLY #051203-4-1 (REV J)		
	Assembly, Front Panel	051158-4-3	1
	Assembly, Rear Panel	051158-4-2	1
A101	Assembly, Power Supply	041809-4-9	1
	Assembly, Transformer	051076-4-2	1
	Bracket, Potentiometer	051204-1-1	1
	Rack, Front Card	051005-1	1
	Rack, Rear Card	051005	1
	Bracket, Transformer	051205	1
	Guide, Card	021340-1-2	18
XA14-16, 18-21	Connector, 50-contact	101204	9
C2	Capacitor, 1000 pF	100076	1
C3	Capacitor, .039 µF, 200 V	101347	1

PARTS LIST

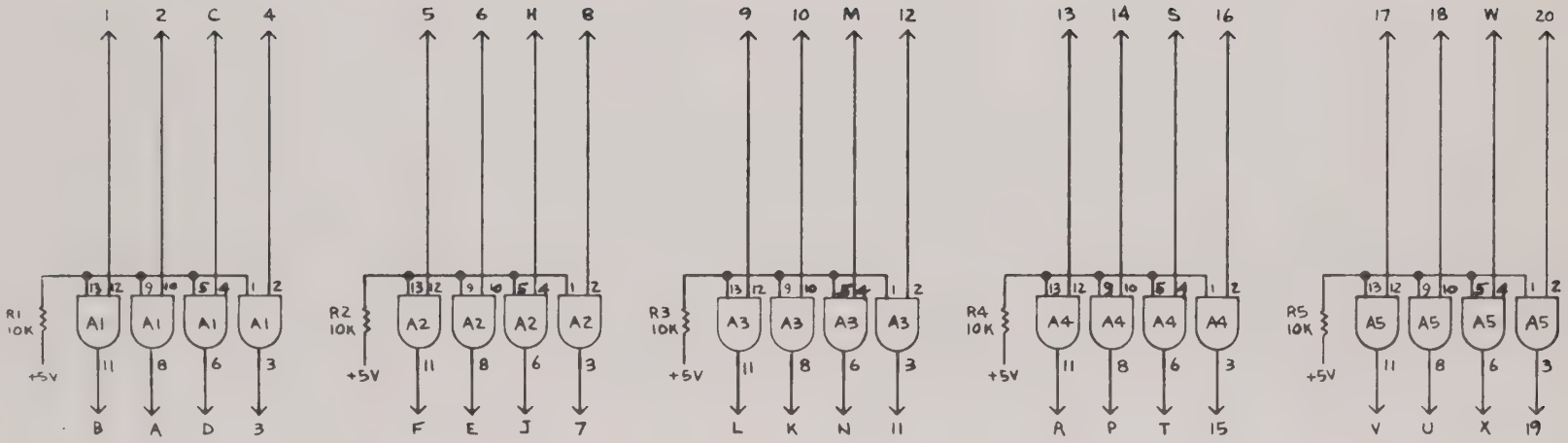
FINAL ASSEMBLY #051207-8-1 (Cont'd)

REF.	DESCRIPTION	SD PART NO.	QTY.
	CHASSIS ASSEMBLY (Cont'd)		
CR1	Diode, 6700	006700	1
R1	Potentiometer, 100 k	102220	1
R2	Resistor, 1.2 k 5%, 1/4 W	101581	1
R3	Resistor, 8.2 k 5%, 1/4 W	101595	1
R4	Resistor, 10 k 5%, 1/4 W	101570	1
R5	Resistor, 20 k 5%, 1/4 W	101607	1
R6	Resistor, 1.8 k 5%, 1/4 W	101602	1
XA101	Connector, Modification	051966-4-1	1
	Gusset, Right	041809-1-2	1
	Gusset, Left	041809-1-1	1
	Spacer, Power Supply	051121-1-1	1
	Connector, 44-contact	101167	1
	Key	102653	2
	Shell, Connector 5-pos	101263	1
	Contact, Male	10282202	5
	FRONT PANEL ASSEMBLY #051158-4-2 (REV B)		
	Panel, Sub-Front	051158	1
	Panel, Nomen	05115702	1
A102	Assembly, Display	041945-4-2	1
M1	Meter	045302	1
XDS1	Socket, Lamp	100899	1
DS1	Lamp, Incadesent 5 V	101130	1
	Lens, White Lamp	10089901	1
S1	Switch, DPST	10231809	1
	Knob	102954	1
	Trim, Strip	04177311	1
	REAR PANEL ASSEMBLY #051202-4-3 (REV C)		
	Panel, Rear	05120203	1
B1	Fan	100038	1
	Screen, Fan	100886	1
J1	Connector, 50-cont	101156	1
J2,4	Connector, 14-pin Cover Plate	021398-1-1	
J3	Connector, 50-pin Cover Plate	031394-1-1	1
J5-10,15,16	Connector, BNC Hole Plug	100952	8
J17	Connector, BNC	101155	1
S12,13	Switch, Cover Plate	05120801	2
S14	Switch, Slide SPDT	102630	1
TB1	Strip, Barrier 4-pos	103069	1

CIRCUIT DESCRIPTION
BUFFER
SCHEMATIC #021535-7-3

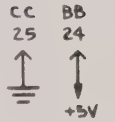
1) GENERAL

This card contains twenty integrated-circuit gates, connected as non-inverting buffers. It is used to buffer the seconds through hours outputs of the Time-of-Day Accumulators. A binary "1" output is 5 V (±0.5 V) 6 kΩ source. A binary "0" output is 0 V (±0.5 V) 15 mA sink.

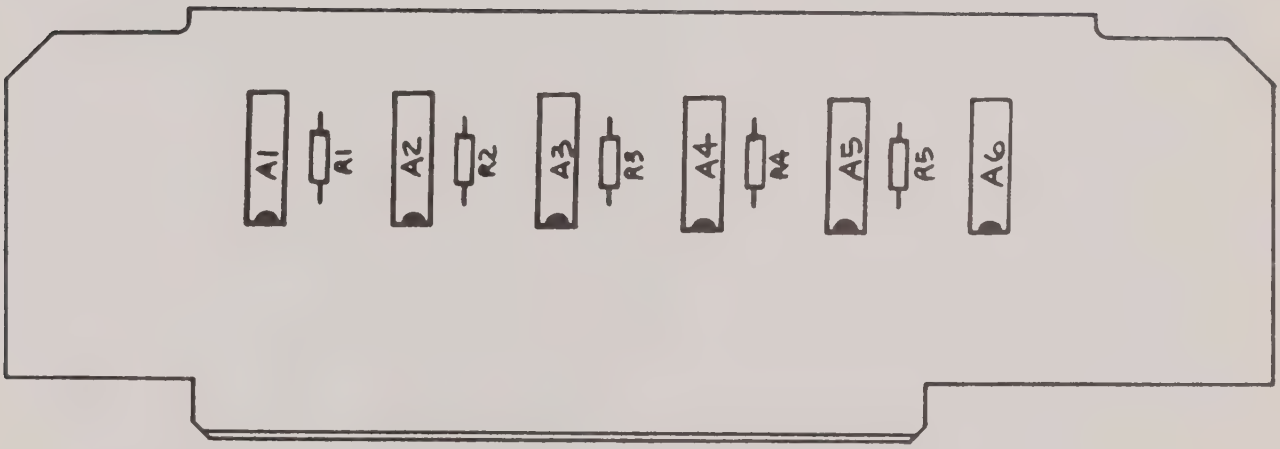


NOTES: (UNLESS OTHERWISE SPECIFIED)

1. RESISTORS ARE IN OHMS, 1/4W, 5%.
2. PIN 14 OF ALL I.C.'S IS CONNECTED TO +5V & PIN 7 " " " " " " GRD.
3. A1 THRU A5 ARE MC1906P.



BUFFER SCHEMATIC #021535-7-3 REV A



BUFFER ASSEMBLY #021535-4-3 REV 1

PARTS LIST

BUFFER ASSEMBLY #021535-4-3 (REV A_n)

REF.	DESCRIPTION	SD PART NO.
	Assembly	021535-4-3
	Schematic	021535-7-3
A1-5	Integrated Circuit, MC1806P	025733
R1-5	Resistor, 10 k 5%, 1/4 W, CC	101570
	Pin, Spring	100752
	Extractor	100865

CIRCUIT DESCRIPTION
TOD ACCUMULATOR
SCHEMATIC #021543-7-3

1) GENERAL

This card successively divides the 1 pps signal to provide outputs which represent seconds through hours. All outputs are buffered, an input inhibit circuit is provided, and the hours dividers are recycled at 23:59:59.

2) DIVIDERS

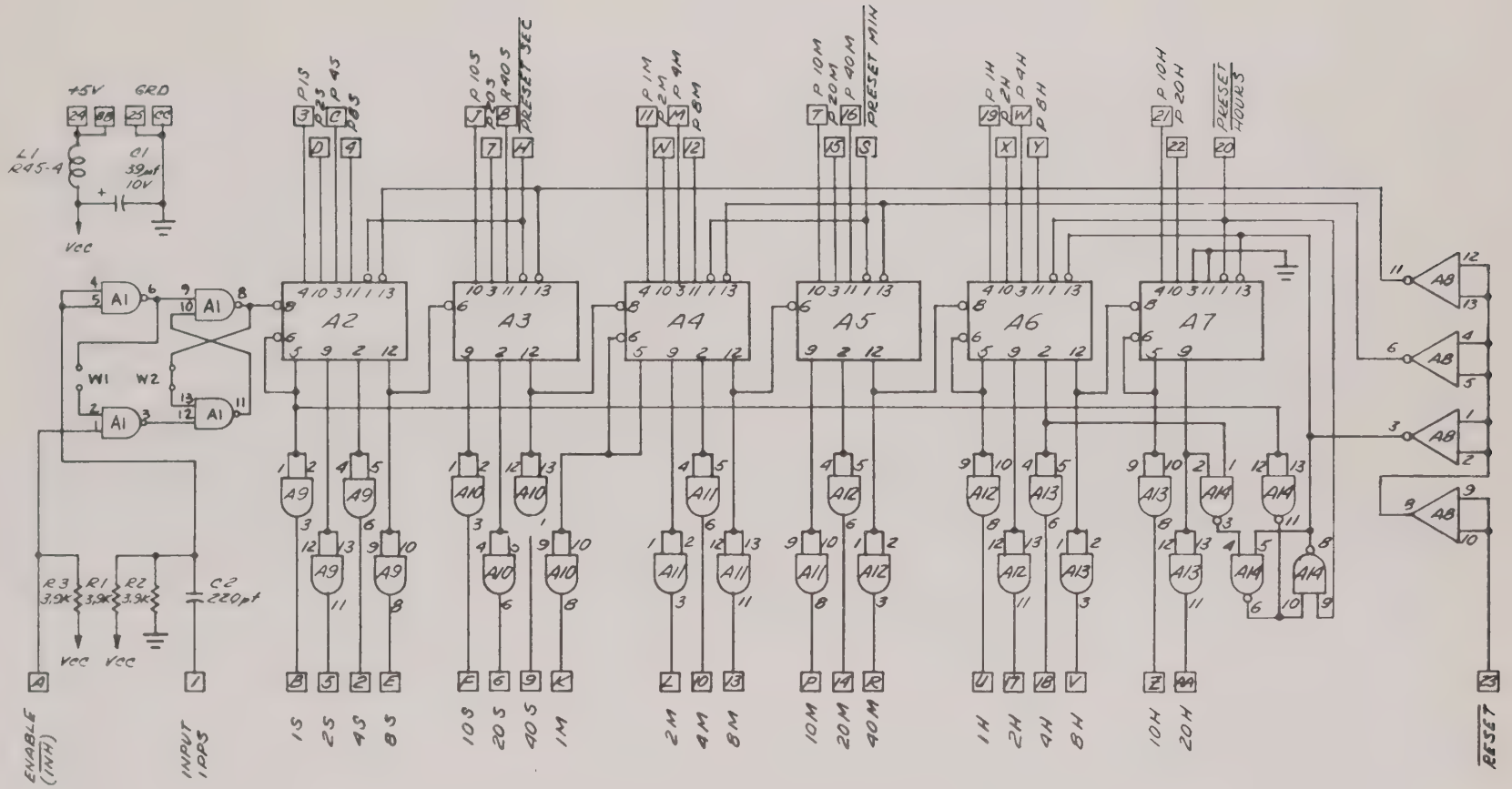
Dividers A2,A4,A6 and A7 divide by 10. Dividers A3 and A5 divide by 6. Each divider has its data inputs connected to the output of a preset thumbwheel switch. Grounding the appropriate preset line will load the preset time into the divider. Inverters A8 are used to buffer the seconds reset lines.

3) INHIBIT CIRCUIT

The Inhibit Circuit is used to stop updating of the accumulator when the front panel MODE Switch is in the HOLD position. Gate A1-6 inverts the 1 pps input. Gates A1-11/A1-8 form an RS flip-flop. Gate A1-3 inverts the $\overline{\text{INHIBIT}}$ line. When the accumulator is updating, A1-11/A1-8 output follows the 1 pps input. When the $\overline{\text{INHIBIT}}$/ENABLE line, pin A, is grounded, the flip-flop will latch with the output high. The output will go low the first time the input is low after the ground has been removed from the $\overline{\text{INHIBIT}}$/ENABLE line.

4) RECYCLE CIRCUIT

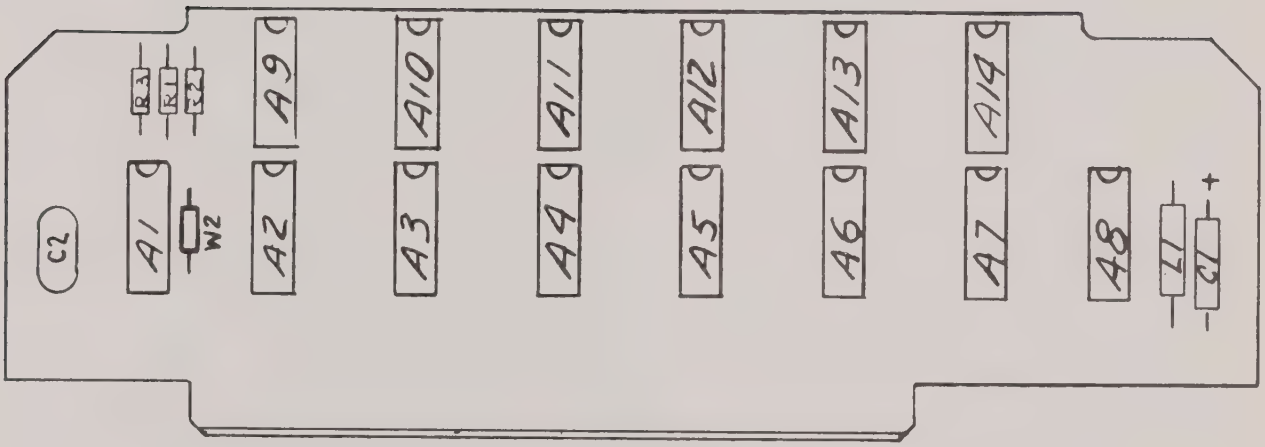
Gates A14-6/A14-8 are connected as an RS flip-flop to control the reset lines of dividers A6 and A7 for recycle at 23:59:59. Gate A14-3 ANDS the 20-hour and the 4-hour outputs to provide a low output at 24-hours. The flip-flop (A14-6/A14-8) output will also go low, resetting A6 and A7 at this time, provided the $\overline{\text{PRESET HOURS}}$ line is high. In this way, recycle is inhibited during preset. Gate A14-11 is wired AND-connected to the flip-flop and maintains the reset pulse for one second. This allows all the flip-flops in the dividers time to reset. Reset may also be initiated from the $\overline{\text{RESET}}$ line via A8-3.



NOTES:

1.) PIN 7 IS CONNECTED TO GRD ON ALL I.C.'S.
2.) PIN 14 " " " Vcc " " "
3.) A2, A4, A6, A7 ARE N8280A
A3, A5 ARE C2125-A
A1, A8, A14 ARE MC846P
A10, A11, A12, A13, A9 ARE MC1806P

TOD ACCUMULATOR SCHEMATIC #021543-7-3 REV B



TOD ACCUMULATOR ASSEMBLY #021543-4-3 REV A

PARTS LIST

TOD ACCUMULATOR #021543-4-3 (REV A_n)

REF.	DESCRIPTION	SD PART NO.
	Assembly	021543-4-3
	Schematic	021543-7-3
A1,8,14	Integrated Circuit, MC846P	019716
A2,4,6,7	Integrated Circuit, N8280A	025722
A3,5	Integrated Circuit, N8288A	025723
A9-13	Integrated Circuit, MC1806P	025733
C1	Capacitor, 39 µF, 10 V	100183
C2	Capacitor, 220 pF	100220
L1	Inductor, R45-4	101313
R1-3	Resistor, 3.9 k 5%, 1/4 W, CC	101601
W2	Jumper, Molded	102879
	Extractor	100865

CIRCUIT DESCRIPTION
TIME BASE
SCHEMATIC #021555-7-27

1) GENERAL

The Time Base Card contains time base circuitry which can be configured in many different ways. The time base usually includes a precision crystal oscillator complete with buffer amplifier and provision for the substitution of an external frequency source. This is followed by a control gate and divider chain.

2) TIME BASE

The Time Base section consists of an unheated crystal, U1, and feedback amplifier Q1. The oscillator output, at pin Y, may be utilized as an external reference or it may be jumpered to pin W for internal use on the card. An external reference signal may be utilized by applying it to pin W in place of the above signal.

The time base signal is applied to the base of voltage-amplifier Q2 (which has a gain of three), isolated, and applied to the base of Q3. Clipper-circuit Q3 provides a 5 V p-p square wave at pin X.

3) DIVIDER CHANGE

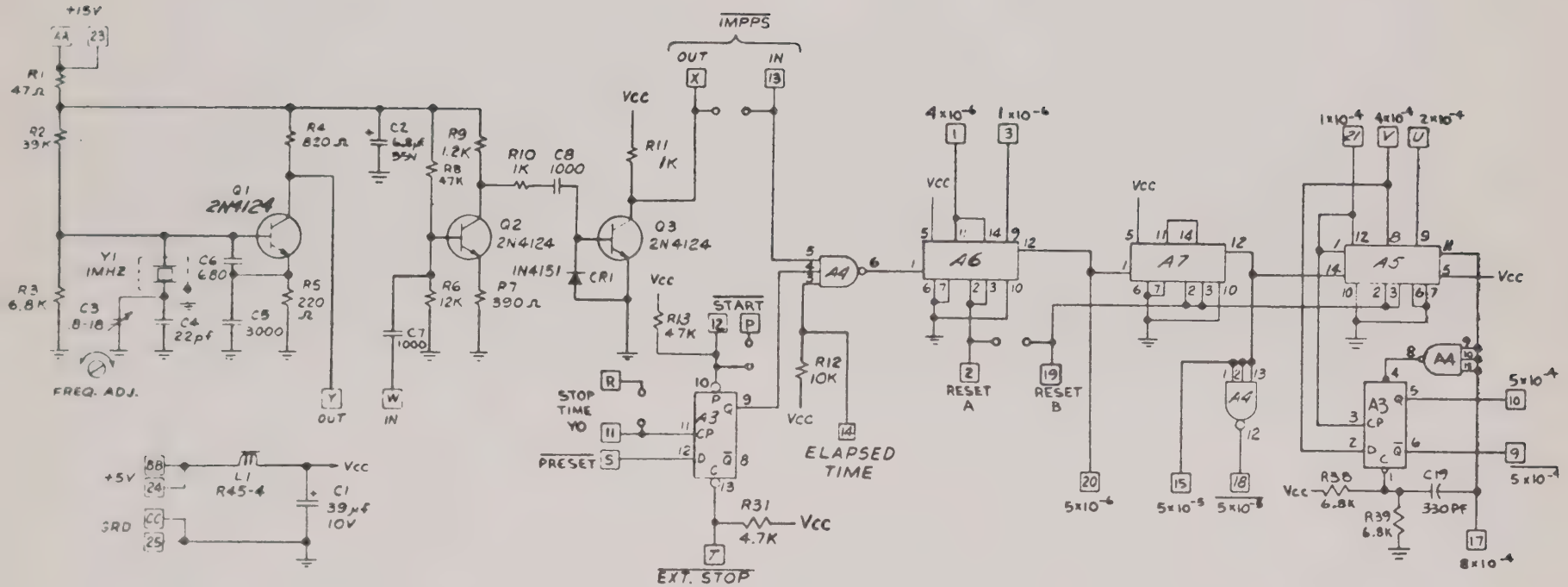
The time base signal at pin X may be fed directly to control gate A4-6 (jumper W1 istalled) or it may be fed to this gate through scale-of-3 pre-divider A2 (jumpers W2 and W3 installed) depending on the time base pulse rate and the application. The time base pulse rate at this point is usually 1 Mpps. Control gate A4-6 has two other inputs. One is the Elapsed Time input from pin 14 and the other is from Stop/Start flip-flop A3-9.

When a Logic 0 (ground) is applied to the External Stop line (pin T), flip-flop A3-9 will generate a Logic 0 which will close gate A4-6 and inhibit the time base input to the divider chain. A positive transition on pin 11 or R, (the Stop time input) will also inhibit the time base if pin S is at ground.

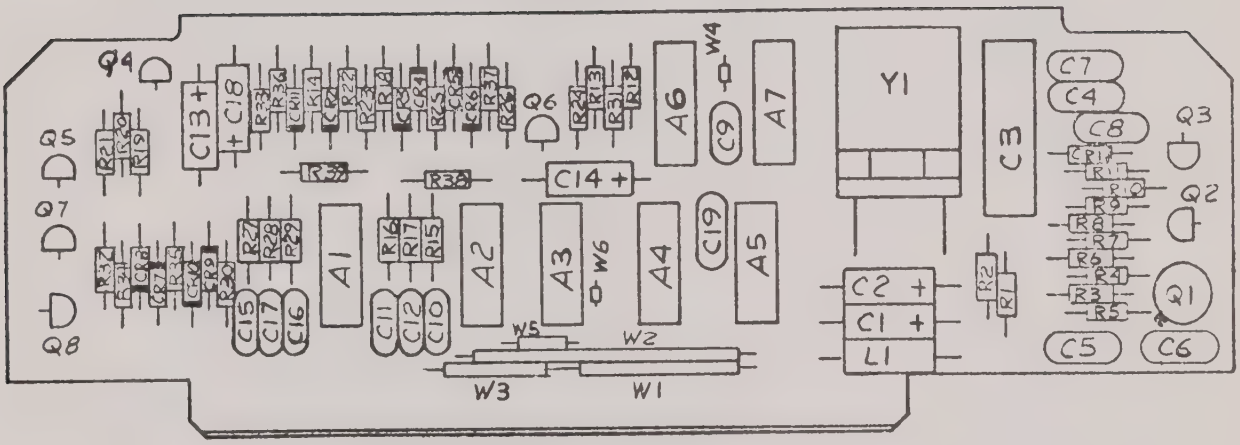
A ground signal on the $\overline{\text{START}}$ pin 12 or P, will clear the inhibit from A4-6.

The divider chain consists of up to three divider chips (A6,A7 and A5) connected in tandum. In most card configurations, these are used as decades. They divide the 1 Mpps time base down to 1 kpps. The first two (A6 and A7) are connected as divide-by-5-then-2 counters. These develop 100 kpps square waves at pins 20 and 15, respectively. The third decade (A5) is connected in the normal divide-by-2-then-5 arrangement. BCD outputs (1-2-4-8) are provided at pins 21,V,U and 17. Flip-flop A3-5 develops complementary 1 kpps square wave outputs at pins 10 and 9.

Pin 2 is the zero reset input to A6. The zero reset inputs to A7 and A5 are connected to pin 19. These two inputs may be jumpered together through W4. These lines must be grounded if not in use.



TIME BASE SCHEMATIC #021555-7-27 REV A



TIME BASE ASSEMBLY #021555-4-1 REV A

PARTS LIST

TIME BASE #021555-7-27 (REV B)

REF.	DESCRIPTION	SD PART NO.
	Assembly (Ref. Assy. Dwg. #021555-4-1)	021555-4-27
	Schematic	021555-7-27
A3	Integrated Circuit, SN7474N	025241
A4	Integrated Circuit, SN7410N	019706
A5-7	Integrated Circuit, SN7490N	025732
C1	Capacitor, 39 µF, 10 V, Tant	100183
C2	Capacitor, 6.8 µF, 35 V, Tant	100182
C3	Capacitor, .8 pF, 35 V, Var	100102
C4	Capacitor, 22 pF, 500 V, Mica	10006801
C5	Capacitor, 3000 pF, 500 V, Dip Mica	100149
C6	Capacitor, 680 pF, 300 V, Dip Mica	10027501
C7,8	Capacitor, 1000 pF, 100 V, Dip Mica	10024301
C19	Capacitor, 330 pF, 500 V, Dip Mica	10027601
CR1	Diode, 1N4151	100385
L1	Inductor, R45-4	101313
Q1-3	Transistor, 2N4124	101377
R1	Resistor, 47 Ω 5%, 1/4 W	101560
R2	Resistor, 39 k 5%, 1/4 W	101561
R3,38,39	Resistor, 6.8 k 5%, 1/4 W	101544
R4	Resistor, 820 Ω 5%, 1/4 W	101567
R5	Resistor, 220 Ω 5%, 1/4 W	101566
R6	Resistor, 12 k 5%, 1/4 W	101565
R7	Resistor, 390 Ω 5%, 1/4 W	101592
R8,13	Resistor, 47 k 5%, 1/4 W	101574
R9	Resistor, 1.2 k 5%, 1/4 W	101581
R10,11	Resistor, 1 k 5%, 1/4 W	101569
R12	Resistor, 10 k 5%, 1/4 W	101570
R31	Resistor, 4.7 k 5%, 1/4 W	101598
	Extractor	100865

CIRCUIT DESCRIPTION
AGC & CYCLE DETECTOR
SCHEMATIC #021569-7-9

1) GENERAL

The AGC & Cycle Detector Card contains two separate and independent circuits. The first circuit (the AGC) provides automatic gain control for the incoming signal. The second circuit generates three control signals: Upper Cycle, Lower Large Cycle and Each Cycle.

2) AGC CIRCUIT

Serial time-code input (from the tape unit, or other source), pin 19, is applied to a voltage divider network which consists of R12 and RET Q1. The bias on the gate of Q1 determines the ratio of the divider network follower providing high input impedance (so as not to load the divider network) and low impedance to drive differential amplifier A5. The input to A5 is applied to the "-" input, pin 2, via R39 for inverting operation.

A5 is provided with negative feedback through R20 for a maximum gain of about 40 dB, and two "roll-off" networks C13-R22, and C12 to ensure stability. Pins T,Y and A are connected by an external jumper except when optional filter networks are used, in which case they are connected between pin T and Y.

The amplified signal is applied to the base of Q4 which controls the emitter voltage of Q3. Q4 and Q3 form a signal peak detection circuit which provides the AGC control voltage to the gate of Q1. The output on pin T is set from 2 V to 2.5 V p-p by adjustment of the AGC potentiometer, R4.

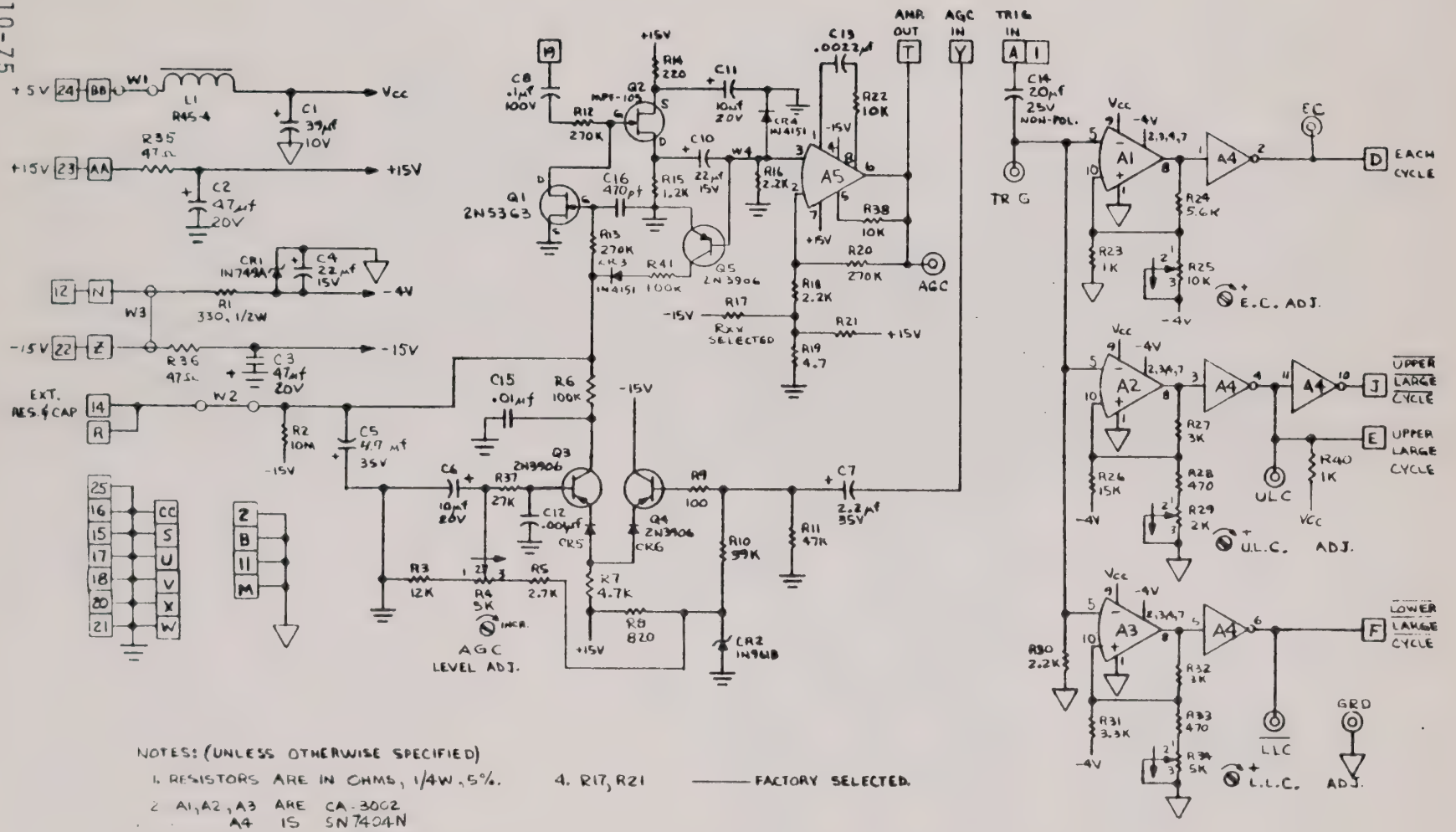
3) CYCLE DETECTOR

The output of amplifier A5 is also applied to three cycle-detector circuits, A1,A2 and A3.

A1 triggers at the zero-axis crossing and will generate a square wave at the input carrier frequency. The hysteresis of this trigger circuit is adjustable by means of the EC potentiometer, R25.

A2 and A3 generate output pulses only upon receipt of a Large Half Cycle; A2, the Upper Large Cycle and A3 the Lawer Large Cycle. These two amplifiers will initiage their signals when the input signal reaches about 75% of the Large Half Cycle amplitude and terminates them when the input signal reaches zero. The trigger points are adjustable by means of the ULC and LLC potentiometers, R29 and R34.

Saturating logic amplifier, A4-2, A4-4 and A4-6, serve to amplify and invert the signals and to provide isolation while A4-8 and A4-12 are used to inhibit the EC output when the $\overline{\text{INH EC}}$ (pin H) is grounded.



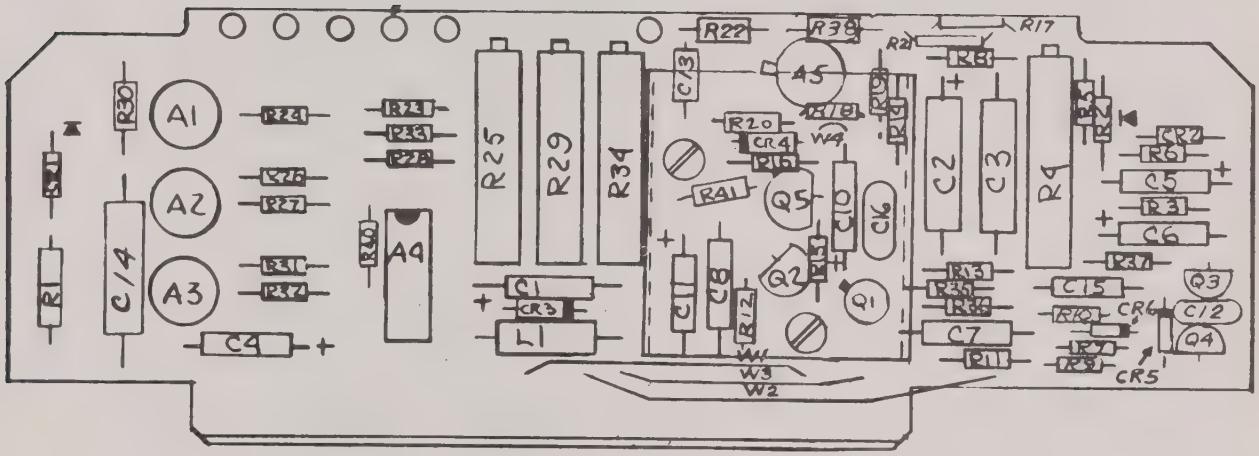
NOTES: (UNLESS OTHERWISE SPECIFIED)

1. RESISTORS ARE IN OHMS, 1/4W, 5%.
2. A1, A2, A3 ARE CA-3002
   A4 IS SN7404N
   A5 IS MC-14396
3. PIN 14 OF A4 IS CONNECTED TO Vcc
   " 7 " " " " " GRD.
4. R17, R21 ——— FACTORY SELECTED.

AGC & CYCLE DETECTOR SCHEMATIC #021569-7-9 REV B

DETAIL A5

TOP VIEW



DETAIL Q1

BOTTOM VIEW

AGC & CYCLE DETECTOR ASSEMBLY #021569-4-9 REV A1

PARTS LIST

AGC & CYCLE DETECTOR #021569-7-9 (REV B)

REF.	DESCRIPTION	SD PART NO.
	Assembly	021569-4-9
	Schematic	021569-7-9
A1-3	Integrated Circuit, CA3002	025701
A4	Integrated Circuit, SN7404N	025779
A5	Integrated Circuit, MC1439G	025729
C1	Capacitor, 39 µF, 10 V	100183
C2,3	Capacitor, 47 µF, 20 V	100186
C4,10	Capacitor, 22 µF, 15 V	100125
C5	Capacitor, 4.7 µF, 35 V	100071
C6,11	Capacitor, 10 µF, 20 V	100063
C7	Capacitor, 2.2 µF, 35 V	100100
C8	Capacitor, .1 µF, 100 V	100141
C12	Capacitor, .001 µF, Disc	100076
C13	Capacitor, .0022 µF	100185
C14	Capacitor, .01 µF, 200 V, Mylar	100168
C15	Capacitor, .01 µF, 200 V	100168
C16	Capacitor, 470 pF	100283
CR1	Diode, 1N749A	100419
CR2	Diode, 1N961B	100395
CR3-6	Diode, 1N4151	100385
L1	Inductor, R45-4	101313
Q1	Transistor, 2N5363	101403
Q2	Transistor, MPF105	101384
Q3-5	Transistor, 2N3906	101378
R1	Resistor, 330 Ω 5%, 1/2 W	101474
R2	Resistor, 10 M 5%, 1/4 W	101564
R3	Resistor, 12 k 5%, 1/4 W	101565
R4,34	Potentiometer, 5 k Beckman 78P	101938
R5	Resistor, 2.7 k 5%, 1/4 W	
R6,41	Resistor, 100 k 5%, 1/4 W	101558
R7	Resistor, 4.7 k 5%, 1/4 W	101598
R8	Resistor, 820 Ω 5%, 1/4 W	101567
R9	Resistor, 100 Ω 5%, 1/4 W	101609
R10	Resistor, 39 k 5%, 1/4 W	101561
R11	Resistor, 47 k 5%, 1/4 W	101573
R12,13,20	Resistor, 270 k 5%, 1/4 W	101769
R14	Resistor, 220 Ω 5%, 1/4 W	101566
R15	Resistor, 1.2 k 5%, 1/4 W	101581
R16,18,30	Resistor, 2.2 k 5%, 1/4 W	101562
R17,21	Factory Select	RXXXXX
R19	Resistor, 4.7 Ω 5%, 1/4 W	101769
R22	Resistor, 10 k 5%, 1/4 W	101570

PARTS LIST

AGC & CYCLE DETECTOR #021569-7-9 (Cont'd)

REF.	DESCRIPTION	SD PART NO.
R23,40	Resistor, 1 k 5%, 1/4 W	101569
R24	Resistor, 5.6 k 5%, 1/4 W	101584
R25	Potentiometer, 10 k Beckman 78P	101918
R26	Resistor, 15 k 5%, 1/4 W	101552
R27,32	Resistor, 3 k 5%, 1/4 W	101548
R28,33	Resistor, 470 Ω 5%, 1/4 W	101625
R29	Potentiometer, 2 k Beckman 78P	101876
R31	Resistor, 3.3 k 5%, 1/4 W	101559
R35,36	Resistor, 4.7 Ω 5%, 1/4 W	101560
R37	Resistor, 27 k 5%, 1/4 W	101587
R38	Resistor, 10 k 5%, 1/4 W	101570
	Extractor	100865

CIRCUIT DESCRIPTION
READER LOGIC
SCHEMATIC #021588-7-1

1) GENERAL

The IRIG Reader Logic Card accepts the Lower Large Cycle ($\overline{LLC}$) and Each Cycle (EC) signals from the AGC & Cycle Detector and detects the ONES, ZEROS and MARKS in the code. It sorts out the BCD time information and loads it into a shift register in 2-digit bytes. These data are transferred, in parallel, to the Time Accumulator by strobe signals generated on the card.

2) FUNCTION

The basic scheme of operation is as follows: When a MARK is detected, the 9-bit shift register (A14) and 1/2 (A13) is cleared and a ONE set in the first bit position. Also, the "Y" Counter A10 is advanced one.

When the second MARK of the couble MARK is detected, the sequence is changed so that the "Y" Counter is set to ZERO if it was not already at ZERO. It is not advanced for this MARK, nor is the shift register cleared. However, the ONE that was entered by the first MARK is shifted one position. The shift register is now advanced one position for each binary bit of the time frame. When the ONE that was entered by the first MARK reaches the ninth position, a circuit is set which permits the next shift signal to transfer the information from the register to the seconds section of the Time Accumulator.

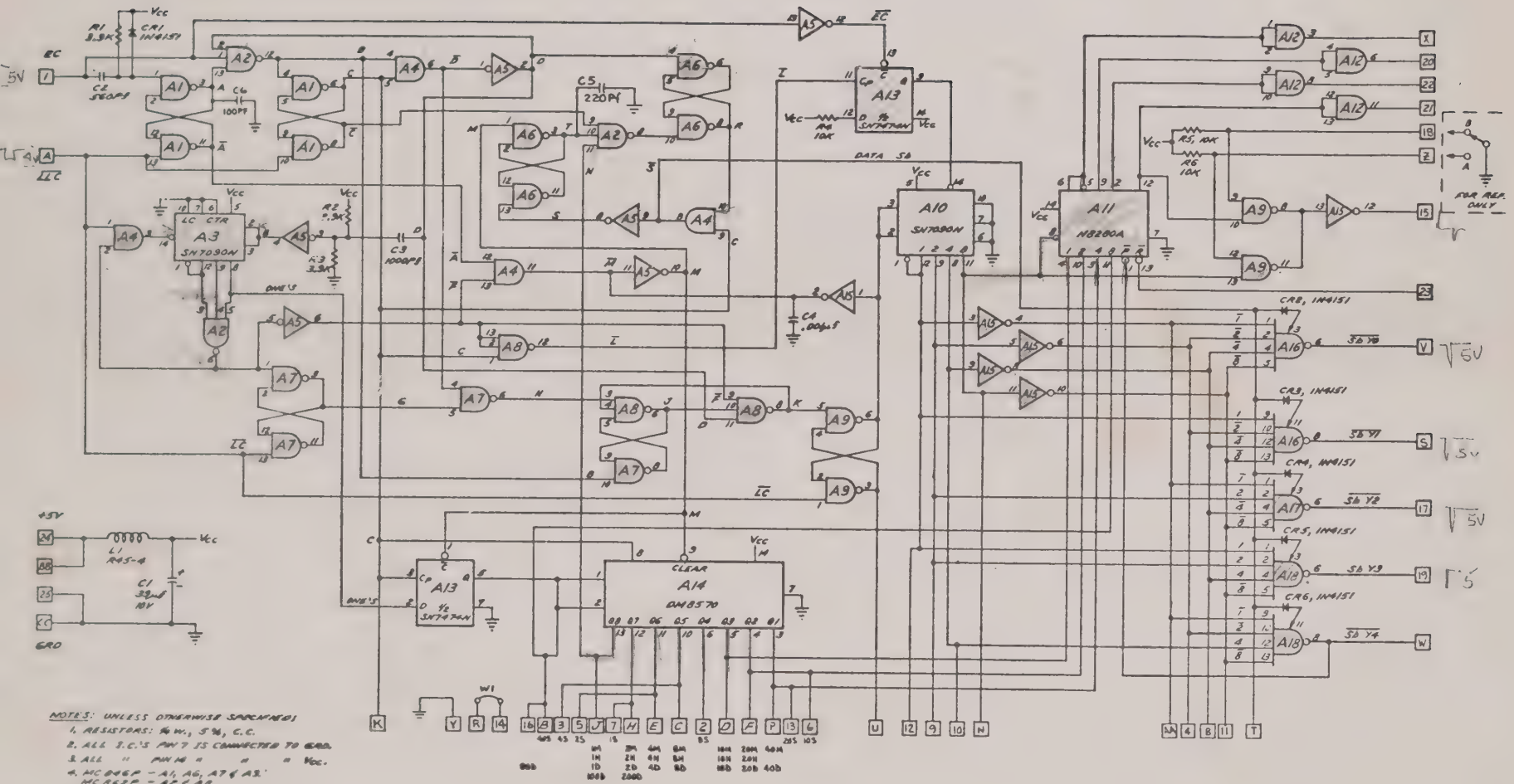
When the next MARK is detected, the register is cleared, a ONE entered and the "Y" Counter advanced one. After 9-bits are shifted into the register the information is transferred to the minutes section of the Accumulator. This cycle of operation is repeated a third time for hours information. If Days is included, 2 additional cycles transfer this information to the Accumulator. The "Y" Counter continues to count MARKS throughout the time frame.

When the first MARK of the next double MARK is detected, it steps the "Y" Counter from 9 to zero advancing the Time Accumulator one second. It is thus updated at the beginning of the frame and will contain the same information (assuming no errors) scanned in during the frame. (The readout does not change during scan-in since the Accumulator is already updated.)

Provision is made through decade A11 and gates on A9, to select 1 pps at pin 15 for the IRIG A and IRIG B codes. Decade A11 is synchronized with the tenths-of-seconds in the IRIG A code by the $\overline{SbY4}$ output from A18-8. Theths-of-seconds are then available at the outputs from A12.

Jumpers are provided to output the ONES signal from A3-8 (pin R), the Clear signal ($\overline{M}$) from A4-11 (pin 14) and the "Y" Counter input from A13-9 (pin M).

8155-9-75

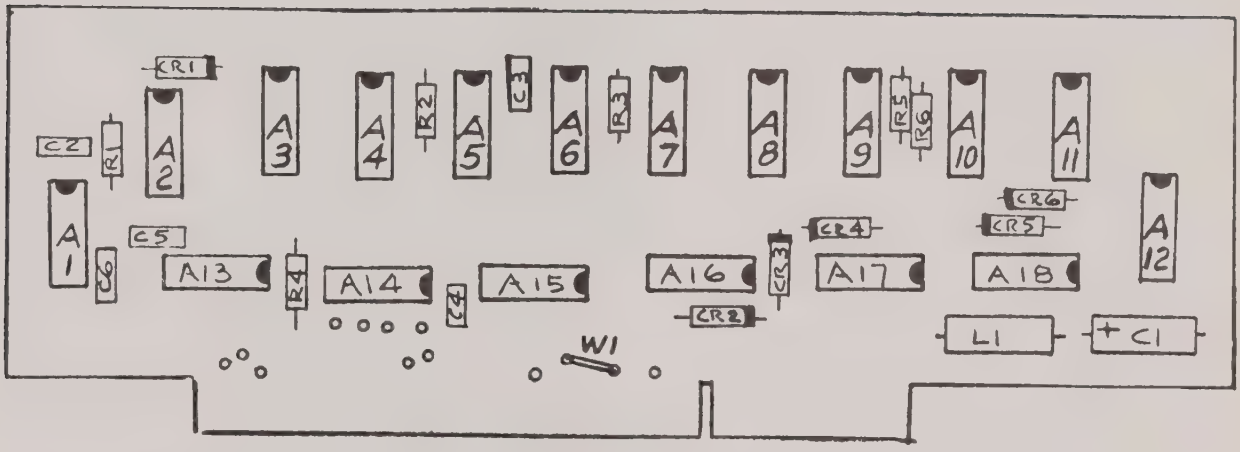


NOTES: UNLESS OTHERWISE SPECIFIED

1. RESISTORS: ¼ W., 5%, C.C.
2. ALL I.C.'S PIN 7 IS CONNECTED TO GRD.
3. ALL " PIN 14 = " = Vcc.
4. MC 846P - A1, A6, A7 & A8.
   MC 847P - A2 & A9.
   MC 1024P - A4 & A10.
   MC 830P - A5 & A15.
   MC 830P - A16, A17 & A18.

5-31

READER LOGIC SCHEMATIC #021588-7-1 REV B



READER LOGIC ASSEMBLY #021588-4-1 REV C

PARTS LIST

READER LOGIC #021588-4-1 (REV A_n)

REF.	DESCRIPTION	SD PART NO.
	Assembly	021588-4-1
	Schematic	021588-7-1
A1,6,7,9	Integrated Circuit, MC846P	019716
A2,8	Integrated Circuit, MC862P	019719
A3,10	Integrated Circuit, SN7490N	025732
A4,12	Integrated Circuit, MC1806P	025733
A5,15	Integrated Circuit, MC836P	025704
A11	Integrated Circuit, N8280A	025722
A13	Integrated Circuit, SN7474N	025241
A14	Integrated Circuit, DM8570	025751
A16-18	Integrated Circuit, MC830P	019712
C1	Capacitor, 39 µF, 10 V	100183
C2	Capacitor, 560 pF, Mica	100222
C3	Capacitor, .001 µF, DM15	100243
C4	Capacitor, .001 µF, Disc	100076
C5	Capacitor, 220 pF, DM15	100220
C6	Capacitor, 100 pF	100173
CR1-6	Diode, 1N4151	100385
L1	Inductor, R45-4	101313
R1-3	Resistor, 3.9 k 5%, 1/4 W	101601
R4-6	Resistor, 10 k 5%, 1/4 W	101570
	Extractor	100865

CIRCUIT DESCRIPTION
MINOR COUNTER
SCHEMATIC #021632-7-4

1) GENERAL

The Minor Counter Card can provide up to 3 serial decades with common reset, parallel preset and 2 sets of buffered, parallel BCD outputs. Provision is made to gate one set of BCD outputs in three 4-bit bytes. The input may be either ac or dc-coupled and fed to the first decade through an update inhibit circuit. A days recycle circuit can be added which may be programmed to reset the accumulator to 001 at the end of 365 or 366 days. Provision is included for 3 output pulse rates with 10% duty cycle which may be supplied in place of the days recycle circuit.

2) DECADE DIVIDERS

The up to 3 decade dividers are connected in tandum. Each is provided with parallel BCD data inputs which may be used to load preset information when the associated data strobe ($\overline{\text{PRESET}}$) line is grounded. W1 and W2 jumpers permit the data strobe associated with the center decade (A4) to be wired in common with the data strobe input to A1, the first decade or A6, the third. The decade zero-reset inputs are wired in common through buffers on A8 to pin 23. The parallel BCD outputs from each decade are wired to output pins through 2 sets of buffers.

3) OUTPUT BUFFERS

The BCD output buffers may be inverting or noninverting. One of the 2 sets (A10,A13 and A15) can be gated by inputs through pins L,K and J, respectively. These gate lines are buffered by inverters on A11.

4) INPUT INHIBIT CIRCUIT

This circuit allows the presence of a ground on pin H to inhibit input signals on pin F from updating the accumulator. Gate A2-6 inverts and buffers the input. Gates A2-11 and A2-8 form an RS flip-flop.

A2-3 gates the $\overline{\text{INHIBIT}}$ line and the inverted input. When the accumulator is updating, flip-flop A2-8,11 output follows the input. When the $\overline{\text{INHIBIT}}$ line, pin H, is grounded the flip-flop will latch with the output high. The output will go low the first time the input is low after the ground has been removed from the $\overline{\text{INHIBIT}}$ line.

5) DAYS RECYCLE CIRCUIT

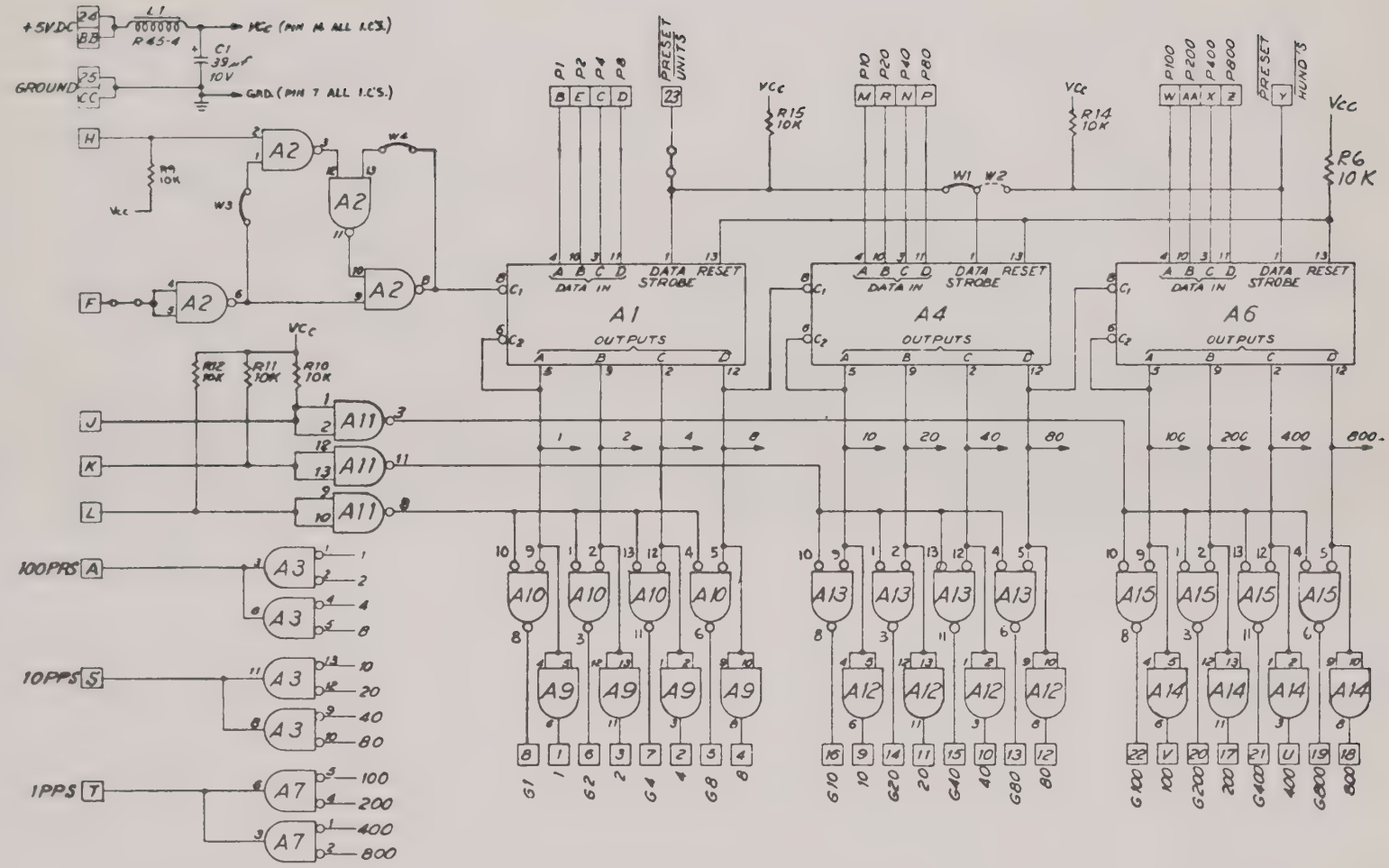
Gate A5-6 is a 4-input NAND gate with an expander input. The connection of diodes CR1-CR3 gives the gate 7-inputs. If recycle at 366 is desired, pin T is connected to Vcc. If recycle at 367 (for Leap Year) is desired, pin T is connected to pin 1 (the one day output). Pin S is always connected to the 2-day output. At the selected count, the output of A5-6 will go low triggering one-shot A8-11,6. The one-shot output is a negative goind pulse (from +5 to 0 V). The leading edge of the pulse (ac-coupled into A8-8) causes the 3 dividers to reset to

000. The trailing edge of the pulse (which is positive going) is ac-coupled into A5-8 where it is inverted and used to input one count to the first decade. The resulting accumulator contents are 001.

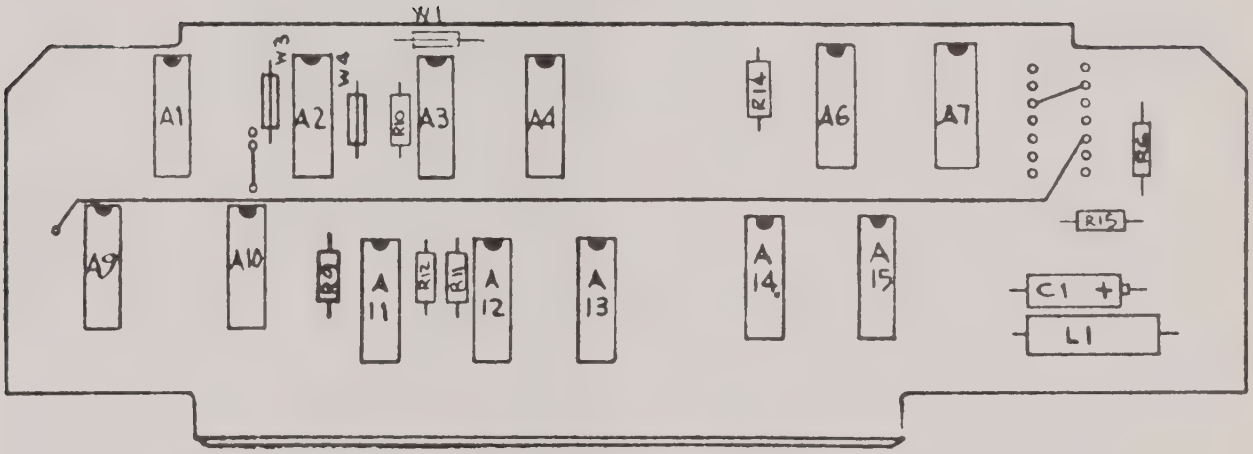
6) OUTPUT PULSE RATES

Three sets of gates are used to produce three 10% duty cycle pulse rates. Each pulse goes high when the 4-outputs from the corresponding decades are low (leading edge on time). The pulse remains up until the output of the decade is 001. Thus, the pulse is high 10% of the time. The output is a 5 V logic level behind 5 kΩ.

The pulse rate outputs are fed to pins A,S and T which are used for units preset and days recycle inputs on other configurations of the card. Chip A5 is removed when the rate outputs are supplied.



MINOR COUNTER SCHEMATIC #021632-7-4 REV A



MINOR COUNTER ASSEMBLY #021632-4-4 REV A

PARTS LIST

MINOR COUNTER #021632-4-4 (REV A_n)

REF.	DESCRIPTION	SD PART NO.
	Assembly	021632-4-4
	Schematic	021632-7-4
A1,4,6	Integrated Circuit, N8280P	025722
A2,11	Integrated Circuit, MC846P	019716
A3,7	Integrated Circuit, MC1810P	025735
A9,12,14	Integrated Circuit, MC1806P	025733
A10,13,15	Integrated Circuit, MC1808P	025734
C1	Capacitor, 39 µF, 10 V	100183
L1	Inductor, R45-4	101313
R6,9-12,14, 15	Resistor, 10 k 5%, 1/4 W	101570
W1,3,4	Jumper, Molded	102879
	Extractor	100865

CIRCUIT DESCRIPTION
CONTROL LOGIC
SCHEMATIC #021654-7-1

1) GENERAL

The main function of the Control Logic circuitry is to control the synchronization of the time code generator section on the basis of an evaluation of the quality of the data derived from the input reference time code.

2) SYNC AND LOAD OUTPUTS

Three sync signals are derived from the differentiated "on time" trailing edge of the one-pulse-per-frame (1 ppF) input from the Reader Logic. These are gated to the Time Base and Minor Counter when all conditions are met for accepting the reference code. The first, through pin Y, resets the Time Base; the second (pin Z) resets the first 2-decades in the Minor Counter and the third (pin X) resets the 3-decade in the Minor Counter when reading IRIG B. This last sync output is replaced by the Load A output (pin V) when reading IRIG A.

The 2 load signals at pins V and 7 are derived from the differentiated trailing edge of the Strobe signal which is, in turn, derived from the Reader Logic. The Strobe is gated during Y9 time. Load A (pin V) presets tenths-of-seconds into the third decade of the Minor Counter when referenced to the IRIG A code. Load B (pin 7) presets TOD and Days data stripped from the reference code into the TOD and Days Accumulators. These signals are also gated only when the reference code is of acceptable quality.

3) PRESET OUTPUT

The preset output at pin AA is the ungated version of the load signals described above. It commands the loading of raw reference code time data into the intermediate accumulator formed from decade U7 (tenths-of-seconds) and similar circuits on the TOD and Days Error Detector Cards. This intermediate, or auxiliary, accumulator is loaded each time frame regardless of the status of the error detector circuits. It is maintained "on time" by Update input signals.

4) TIME DATA COMPARATOR

The time data comparator consists of U6 and similar circuits on the Error Detector Cards. It compares the parallel time data output from the Reader Logic with the contents of the intermediate accumulator. The coincidence output from each comparator gate is tied to a common bus labeled COIN which is fed through gates to the Good Frame Counter U1.

5) GOOD FRAME COUNTER

The Good Frame Counter, U1, counts Strobe pulses provided the COIN bus is positive at the time the Strobe occurs. This will be the case if the time data stripped from the reference code during a frame matches the contents of the intermediate accumulator.

U1 counts a selected number of consecutive "good" frames then locks up. The number of good frames is determined by decoding gates on U8 and U10 which are selected through inverters on U9 from pins H,J and M. The number is usually set at 3. If a bad frame is encountered, U1 is reset and a new count started.

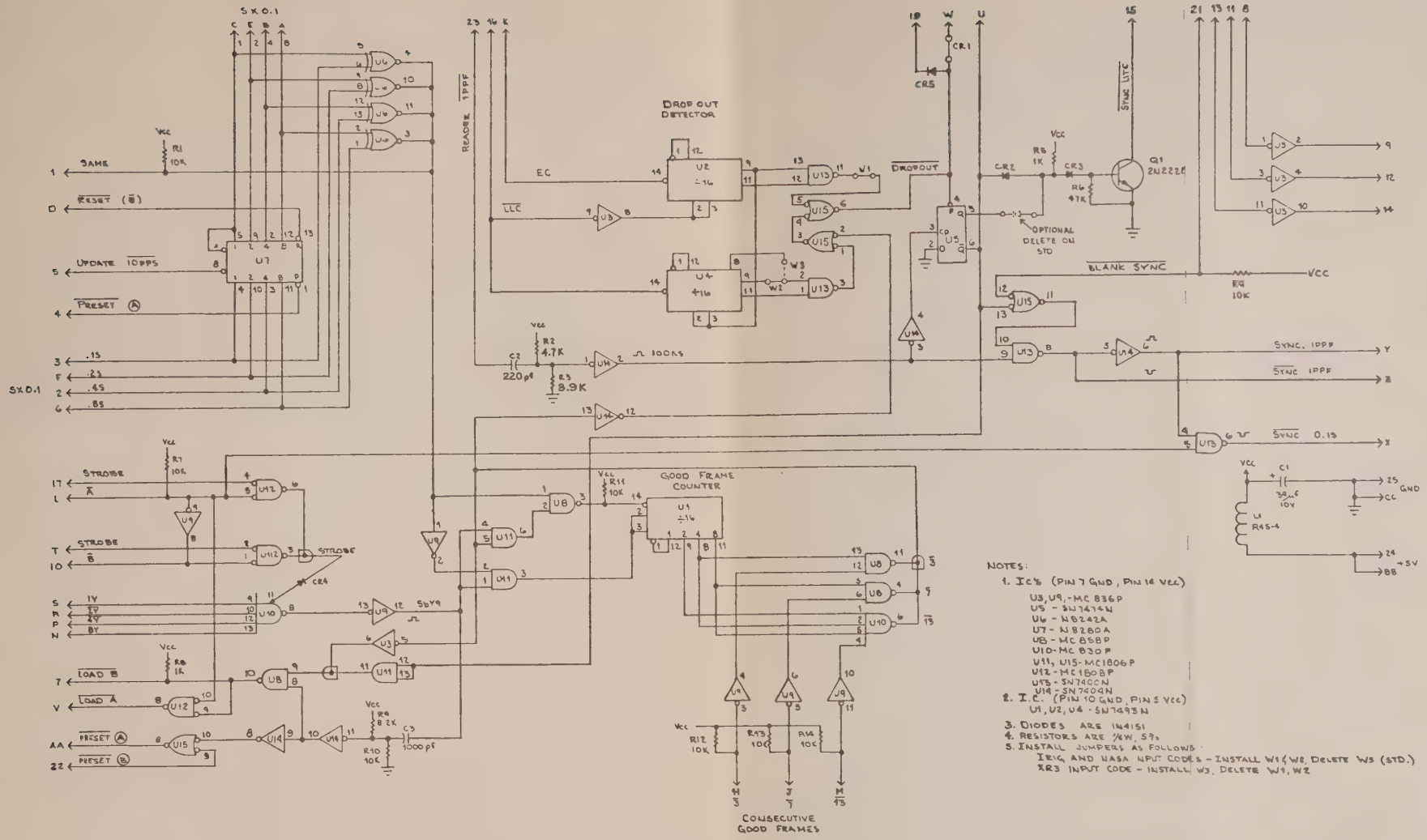
As long as U1 is counting, the sync and load outputs are disabled. When it enters the "locked" state, these signals are gated through, provided no dropout condition exists.

6) DROPOUT DETECTION

A dropout signal may be generated as a result of loss of the reference signal carrier or the loss of modulation. The former is developed on the Input Logic Card. The latter is the output from the modulation detector formed from counters U2 and U4. When a dropout occurs, flip-flop U5 is preset closing the sync and load signal gates (U13-8 and U8-10) and turning off the sync lamp through driver Q1.

The modulation detector functions as follows: U2 counts EC pulses. It is reset by each $\overline{\text{LLC}}$ input pulse through U3-8. U4 counts $\overline{\text{LLC}}$ pulses and is reset when U2 reaches a count of 2. Since the negative going transition of the EC signal occurs before the associated $\overline{\text{LLC}}$ transition, U2 goes to a count of 1 between $\overline{\text{LLC}}$ pulses. Thus, it reaches a count of 2 (resetting U4) even if there is only one small cycle between two groups of large cycles. Digital filtering within the REader Logic accepts 1,2 or 3 large cycles for a 0; 3,4 or 5 large cycles for a 1 and 7,8 or 9 for a marker. This means that from 1 to 9 consecutive la large or small cycles are acceptable but 10 or more are not. A gate associated with each counter decodes the count of 10 presetting flip-flop U5.

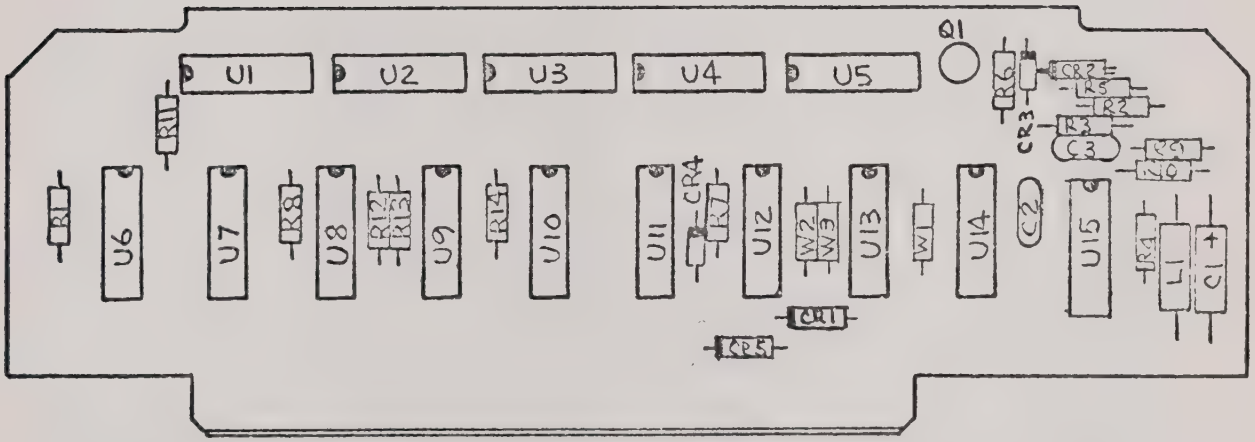
The sync outputs are blanked when the $\overline{\text{blank sync}}$ line from pin 21 goes low. This will occur whenever the frame marker is not precisely the correct length. See Input Logic Card description.



NOTES:

1. IC's (PIN 7 GND, PIN 14 VCC)
   U3, U9, - MC 836P
   U5 - SN7474N
   U6 - NB242A
   U7 - NB260A
   U8 - MC 858P
   U10 - MC 830P
   U11, U15 - MC1806P
   U12 - MC1608P
   U13 - SN7400N
   U14 - SN7404N
2. I.C. (PIN 10 GND, PIN 5 VCC)
   U1, U2, U4 - SN7493N
3. DIODES ARE IN4151
4. RESISTORS ARE ¼W, 5%
5. INSTALL JUMPERS AS FOLLOWS:
   IRIG AND NASA INPUT CODES - INSTALL W1 & W2, DELETE W3 (STD.)
   XR3 INPUT CODE - INSTALL W3, DELETE W1, W2

CONTROL LOGIC
SCHEMATIC #021654-7-1 REV B



CONTROL LOGIC ASSEMBLY #021654-4-1 REV A,

PARTS LIST

CONTROL LOGIC #021654-4-1 (REV B)

REF.	DESCRIPTION	SD PART NO.
	Assembly	021654-4-1
	Schematic	021654-7-1
C1	Capacitor, 39 µF, 10 V	100183
C2	Capacitor, 220 pF, 500 V, DM15	100220
C3	Capacitor, 1000 pF, 100 V	100243
CR1	Jumper, Molded	102879
CR2-5	Diode, 1N4151	100385
Q1	Transistor, 2N2222	101347
R1,4,7,10-14	Resistor, 10 k 5%, 1/4 W	101570
R2	Resistor, 4.7 k 5%, 1/4 W	101598
R3	Resistor, 3.9 k 5%, 1/4 W	101601
R5,8	Resistor, 1 k 5%, 1/4 W	101569
R6	Resistor, 47 k 5%, 1/4 W	101574
R9	Resistor, 8.2 k 5%, 1/4 W	101595
U1,2,4	Integrated Circuit, SN7493N	025715
U3,9,14	Integrated Circuit, MC836P	025704
U5	Integrated Circuit, SN7474N	025241
U6	Integrated Circuit, N8242A	025755
U7	Integrated Circuit, N8280A	025722
U8	Integrated Circuit, MC858P	025748
U10	Integrated Circuit, MC830P	019712
U11,15	Integrated Circuit, MC1806P	025733
U12	Integrated Circuit, MC1808P	025734
U13	Integrated Circuit, MC846P	019716
W1,2	Jumper, Molded	102879
	Extractor	100865

CIRCUIT DESCRIPTION
TOD ERROR DETECTOR
SCHEMATIC #021655-7-2

1) GENERAL

The TOD Error Detector Card contains a TOD accumulator which is updated on time; a parallel storage register for storing hours, minutes and seconds bytes stripped from the reference time code; a parallel comparator for comparing their contents and an hours recycle circuit.

2) TOD ACCUMULATOR

Dividers U,U8,U14 and U17 divide by 10. Dividers U5 and U11 divide by 6. Each divider has data inputs which are connected to the storage register as the source of preset information. Grounding the preset input (pin 7) loads the storage register contents into the accumulator. Each divider also has parallel outputs which are externally wired to the main TOD Accumulator Card. These lines, along with the storage register outputs, are also connected to the parallel comparator.

3) STORAGE REGISTER

The storage register consists of quad latch chips U4,U7,U10,U13,U16 and U19. These are loaded in 3-bytes of hours, minutes and seconds from the Reader Logic as this information is stripped from the reference input code. The units digits are strobed through inverters on U1. The tens digits are strobed through inverters on the Control Logic Card.

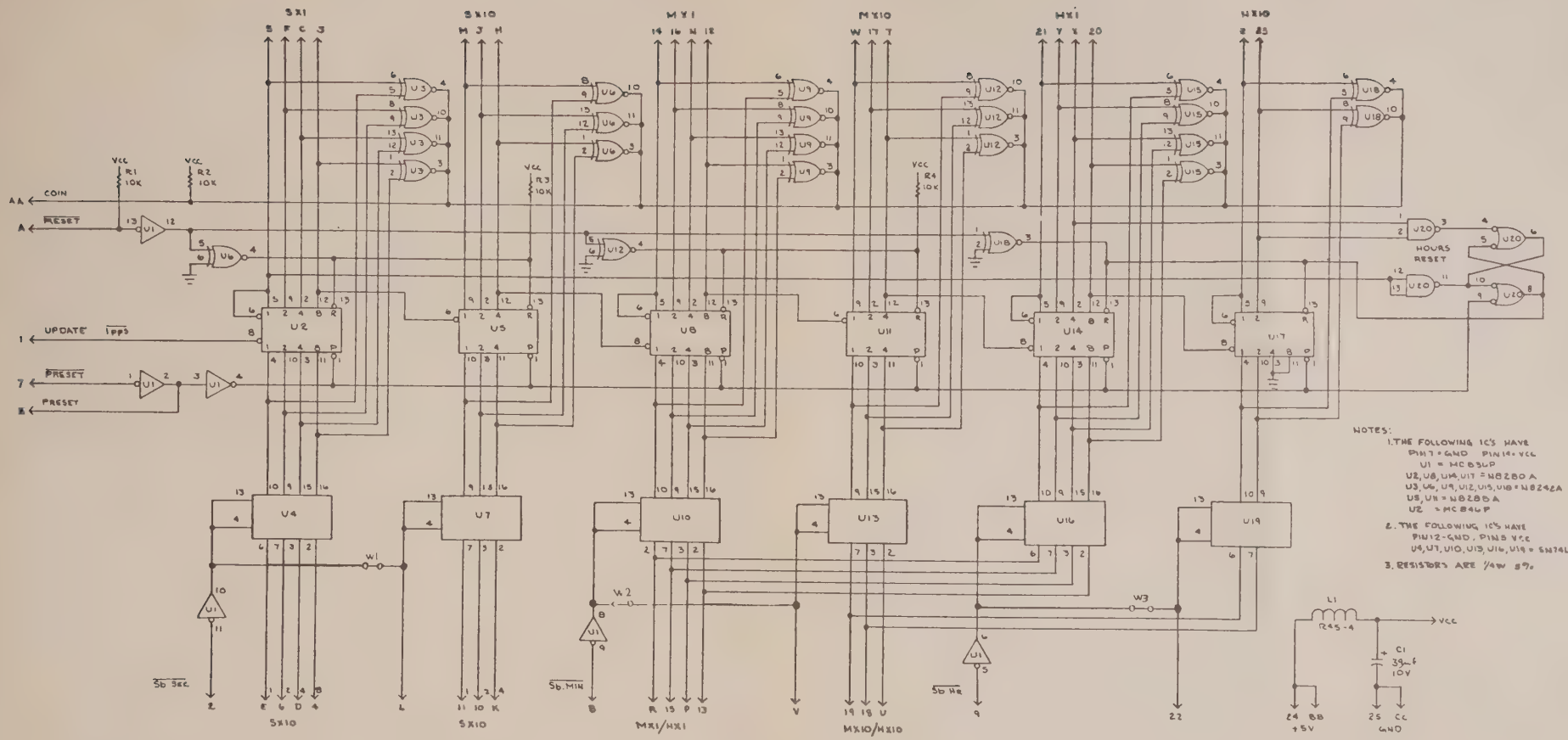
4) COMPARATOR

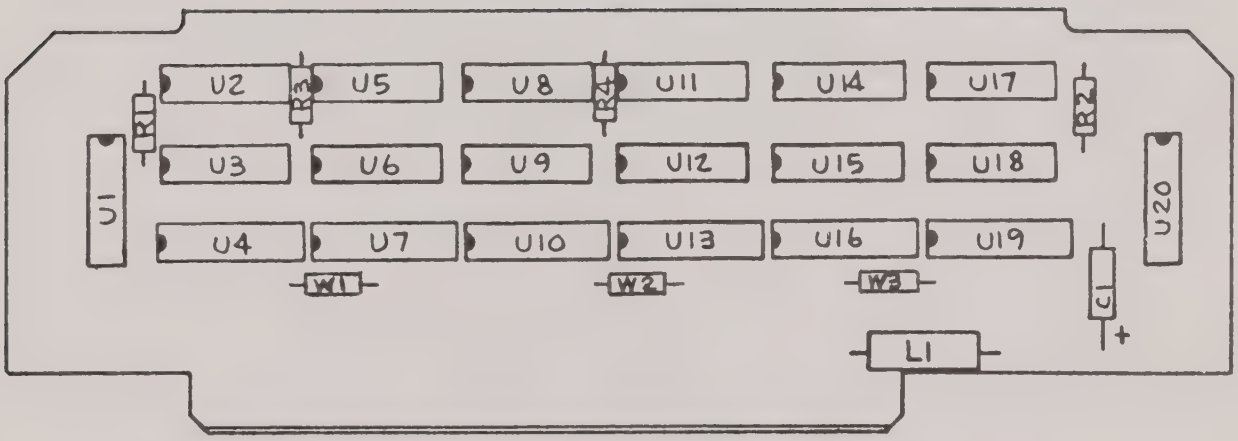
The parallel comparator is formed from gates on U3,U6,U9,U12,U15 and U18. The output from each gate is tied to a common coincidence bus connected to pin AA. This line goes positive when all bits in the accumulator match the corresponding bits in the storage register.

Operation is as follows: A strobe signal developed on the Control Logic Card samples the comparator output during Y9 time after the Reader data have been loaded into the storage register. On the trainling edge of this strobe, these data are transferred into the accumulator by the preset input. (If the system is in sync with the reference code, the accumulator will already contain this same information.) At the beginning of the next frame (IRIG B code) the accumulator is updated by one count (1 pps input to pin 1), the new frame data from the Reader are loaded into the storage register and the new comparison is sampled by the Control Logic strobe. The cycle is then repeated. Operation with an IRIG A reference code is identical with the exception that ten samples are made for each update of the accumulator.

5) HOURS RECYCLE

An hours recycle circuit is formed from gates on U20. This circuit automatically resets the hours decades (U14 and U17) at 24 hours. Reset of the entire accumulator to 00:00:00 may be accomplished by grounding the reset input at pin A.


SX1
SX10
MX1
MX10
HX1
HX10
COIN
RESET
UPDATE 1pps
PRESET
PRESET
HOURS RESET
NOTES:
1. THE FOLLOWING IC'S HAVE PIN 7 = GND PIN 14 = VCC
U1 = MC 853P
U2, U3, U4, U5, U7 = MB2804A
U3, U6, U9, U12, U15, U18 = MB2424A
U8, U11 = MB2804A
U2 = MC 846P
2. THE FOLLOWING IC'S HAVE PIN 12 = GND, PINS VCC
U4, U7, U10, U13, U16, U19 = SN74L75N
3. RESISTORS ARE 1/4W 5%
TOD ERROR DETECTOR
SCHEMATIC #021655-7-2



TOD ERROR DETECTOR ASSEMBLY #021655-4-2

PARTS LIST

TOD ERROR DETECTOR #021655-4-2 (REV A_1)

REF.	DESCRIPTION	SD PART NO.
	Assembly	021655-4-2
	Schematic	021655-7-2
C1	Capacitor, 39 µF, 10 V	100183
L1	Inductor, R45-4	101313
R1-4	Resistor, 10 k 5%, 1/4 W	101570
U1	Integrated Circuit, MC836P	025704
U2,8,14,17	Integrated Circuit, N8280A	025722
U3,6,9,12,15,18	Integrated Circuit, N8242A	025755
U4,7,10,13,16,19	Integrated Circuit, SN74L75N	045201
U5,11	Integrated Circuit, N8288A	025723
U20	Integrated Circuit, MC846P	019716
W1-3	Jumper, Molded	102879
	Extractor	100865

CIRCUIT DESCRIPTION
INPUT LOGIC
SCHEMATIC #021674-7-1

1) GENERAL

The Input Logic Card contains: a) the Frame Marker Length Detector; b) the each cycle Dropout Detector and; c) a part of the input level Meter Circuit.

2) FRAME MARKER LENGTH DETECTOR

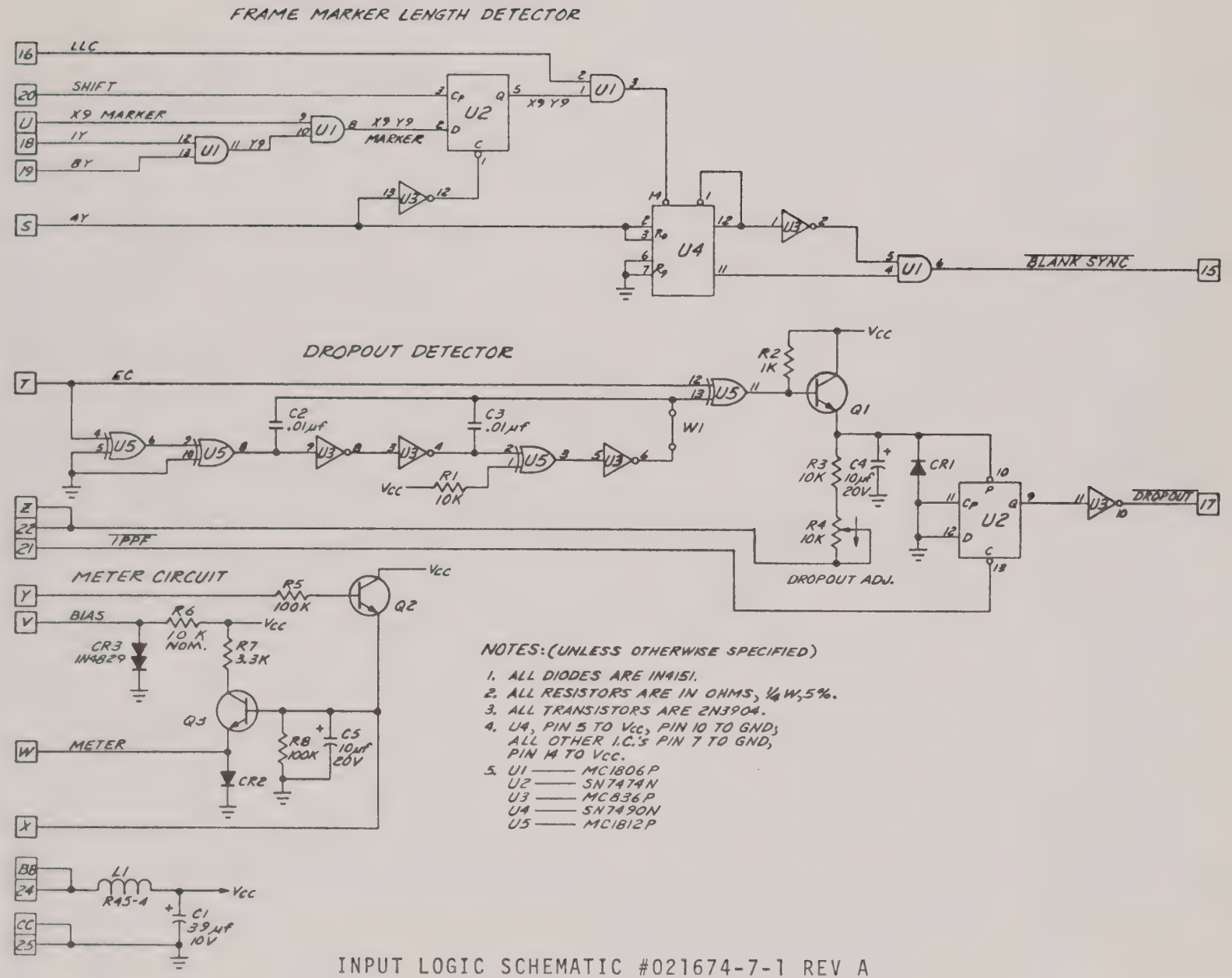
This circuit measures the length of the index mark which occurs at X9Y9 time in the IRIG time code frame by counting $\overline{LLC}$ pulses during the X9Y9 period. If there are not precisely 8 pulses (equivalent to 8 large cycles in the time code) the output at pin 15 goes to ground and the sync pulses developed on the Control Logic Card are blanked.

3) DROPOUT DETECTOR

This circuit detects the presence of the Each Cycle (EC) output from the AGC & Cycle Detector Card. The EC signal is fed through pin T directly to one input to exclusive OR gate U5-11. A delayed version of the EC signal is fed to the other input. The resulting output at U5-11 is a pulse train at twice the EC rate. These pulses are amplified by Q1 and fed to the flip-flop U2-9 and the related network. Capacitor C4 is charged to the "1" level as long as the input pulses are present. The flip-flop is in the reset state having been placed in this condition by the $\overline{1\ ppF}$ input to pin 21. If, however, the pulses vanish, C4 is discharged through R3 and R4 and the flip-flop is set. The output through U3-10 and pin 17 ($\overline{Dropout}$) is fed to the Control Logic Card where it blocks synchronization and turns off the sync lamp.

4) METER CIRCUIT

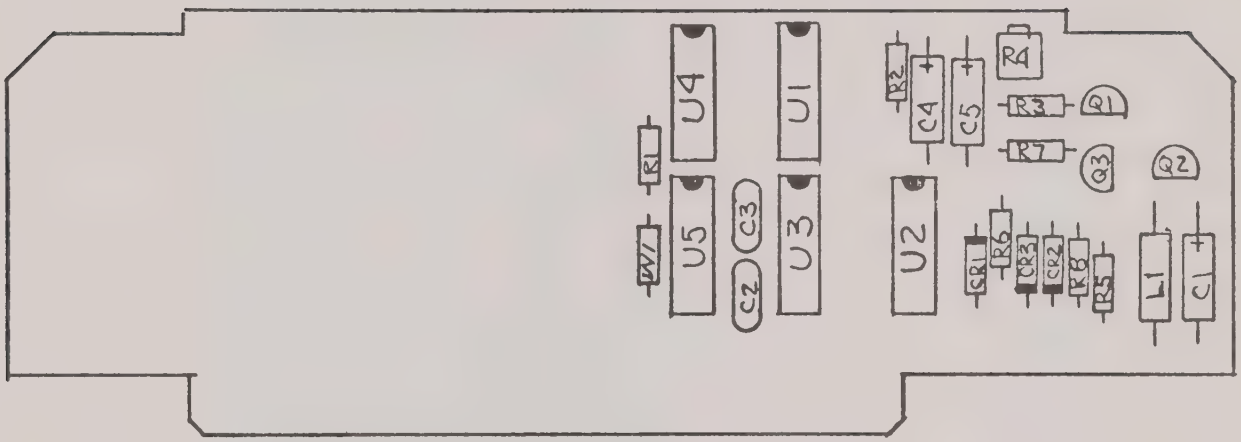
The Meter Circuit develops a voltage which is roughly proportional to the peak of the input reference signal. The amplified input signal is fed to pin Y through the Meter Set potentiometer R1 (See Block Diagram). Capacitor C5, is charged to the positive peak amplitude through Q2 and the meter is driven through Q3.



NOTES: (UNLESS OTHERWISE SPECIFIED)

1. ALL DIODES ARE IN4151.
2. ALL RESISTORS ARE IN OHMS, ¼W, 5%.
3. ALL TRANSISTORS ARE 2N3904.
4. U4, PIN 5 TO Vcc, PIN 10 TO GND; ALL OTHER I.C.'s PIN 7 TO GND, PIN 14 TO Vcc.
5. U1 —— MC1806P
   U2 —— SN7474N
   U3 —— MC836P
   U4 —— SN7490N
   U5 —— MC1812P

INPUT LOGIC SCHEMATIC #021674-7-1 REV A



INPUT LOGIC ASSEMBLY #021674-4-1

PARTS LIST

INPUT LOGIC #021674-4-1 (REV A_2)

REF.	DESCRIPTION	SD PART NO.
	Assembly	021674-4-1
	Schematic	021674-7-1
C1	Capacitor, 39 µF, 10 V, Tant	100193
C2,3	Capacitor, .01 µF, 100 V, Disc	100103
C4,5	Capacitor, 10 µF, 20 V, Tant	100063
CR1,2	Diode, 1N4151	100385
CR3	Diode, 1N4829	100443
L1	Inductor, R45-4	101313
Q1-3	Transistor, 2N3904	101377
R1,3,6	Resistor, 10 k 5%, 1/4 W, CC	101570
R2	Resistor, 1 k 5%, 1/4 W, CC	101569
R4	Resistor, 10 k 5%, 1/2 W	101937
R5,8	Resistor, 100 k 5%, 1/4 W	101558
R7	Resistor, 3.3 k 5%, 1/4 W	101559
U1	Integrated Circuit, MC1806P	025733
U2	Integrated Circuit, SN7474N	025241
U3	Integrated Circuit, MC836P	025704
U4	Integrated Circuit, SN7490N	025732
U5	Integrated Circuit, MC1812P	025736
W1	Jumper, Molded	102879

CIRCUIT DESCRIPTION
POWER SUPPLY
SCHEMATIC #041810-7-9

1) GENERAL

The Power Supply provides 4 regulated dc voltages (±5 V and ±15 V), 5 unregulated dc voltages (±9 V, ±21 V and +210 V) and an 18 V rms time base output at the line frequency. The regulated output voltage levels are adjustable. These outputs are current-limited and are short-circuit-proof to ground. (Note: Overheating may result if a short is maintained over an extended period of time.) Both voltage-sense and sense-return lines are provided for the regulated outputs. These lines are wired to provide regulation at the load. Fuses are provided for the unregulated +21 V and +210 V on the Power Supply Assembly.

Input power is 115/230 V, 48 to 440 Hz at less than 100 watts with nominal line and all outputs fully loaded. (Note: The line frequency may be limited, 48 to 62 Hz unless Option L12 is utilized, by the fan characteristics if a fan is included in the unit.) Input power is fed to transformer T1 through line filter Z1, fuse F1, a front panel power switch and 115/230 select switch S101. The third wire is grounded to the chassis.

The transformer is constructed with split-primary windings which are connected in parallel for 115 V operation and in series for 230 V operation. Selection is made by 115/230 switch S101. (Note: Units are normally shipped in the 115 V configuration with a 2A Slo-Blo fuse, F1. If the unit is converted to 230 V operation, F1 should be changed to 1A Slo-Blo.) Three secondary windings (two with center taps) are provided, one for ±9 V, one for ±21 V and 18 V rms, and the third for +210 V.

2) NONREGULATED SUPPLIES

The +210 V nonregulated supply is developed by the bridge rectifier formed from diodes CR5 through CR8, plus the filter circuit formed from R1,R2 and C5. The resulting output is fed through F2 (0.125A) to P103, pins 18 and V. It is used to drive front panel numerical indicating tubes and is rates at 100 mA.

The ±21 V nonregulated supplies are devloped by bridge rectifier CR1 through CR4 and filtered by C1,C2,C8 and C11. The +21 V output is used internally as the source for the +15 V regulator. It is fed through F3 (1A) to P103, pins 15 and S, where it is available for use as a relay supply. The -21 V output is used internally as the source for the -15 V regulator, and to power both the -15 V and -5 V regulator amplifiers. It is also available at P103, pin 4, for external use. Each of the ±21 V supplies is rated at 0.5A.

The 18 V rms is derived for the secondary winding which provides the ac voltage to develop the ±21 V. This rms voltage is fed through R15 to P103 pins 22 and Z.

The +9 V nonregulated supply is developed by fullwave rectifier CR11, CR12 and filtered by C3,C4 and C10. It is used internally as the sour source for the +5 V regulator, and to power both the -15 V and -5 V regulator amplifiers. It is available at P103, pins 21 and Y, for external use as a lamp supply. It is rated at 4A.

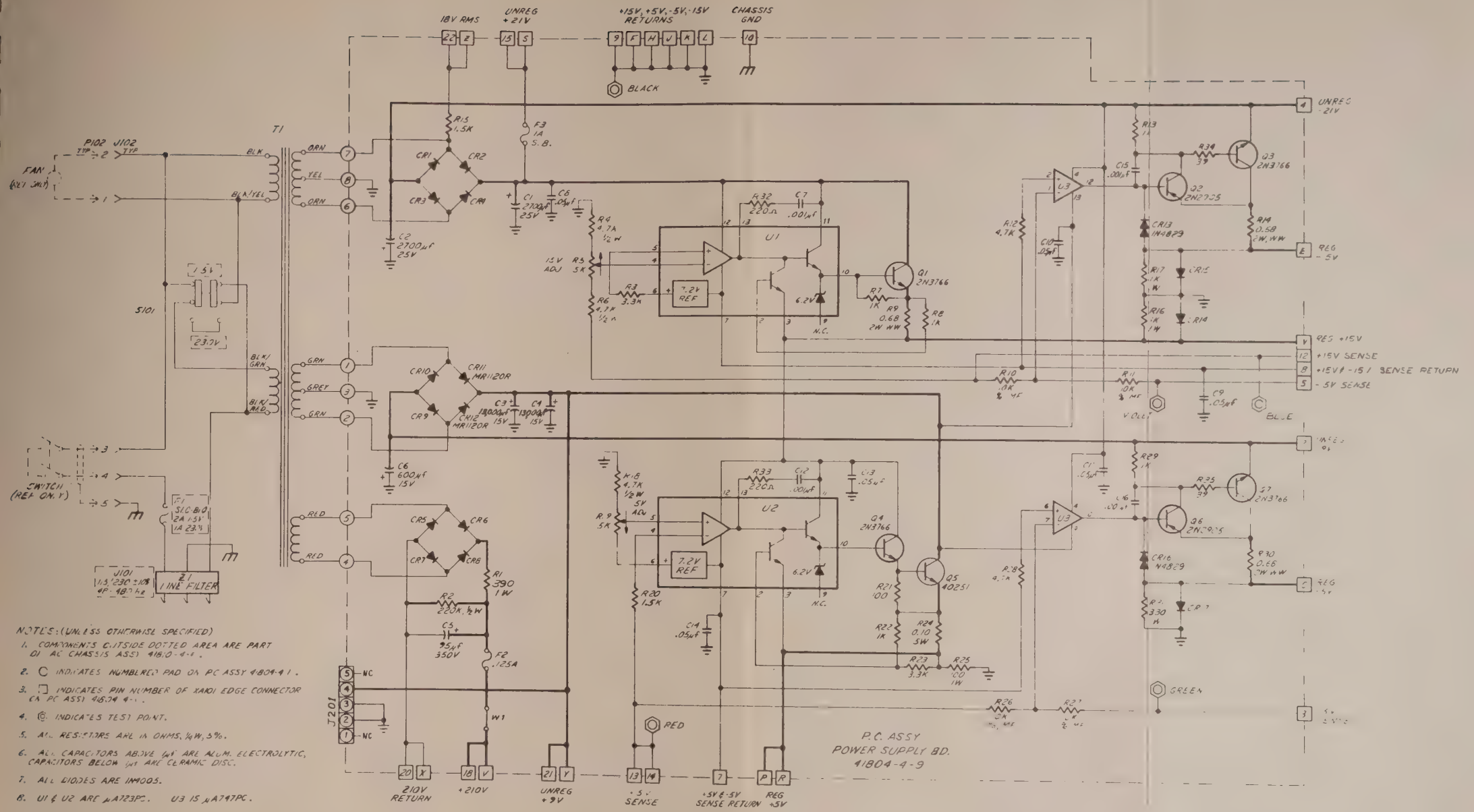
The -9 V nonregulated supply from fullwave rectifier CR9,CR10 and filter C6 is used internally as the source for the -5 V regulator. It is available at P103, pin 2, for external use. It is rated at 0.5A.

3) REGULATED SUPPLIES

The regulated +15 V, 0.5A output at P103, pin N, is established through pass transistor Q1, under the control of regulator U1 and the divider network (R4,R5,R6) between the +15 V SENSE line (P103, pin 12) and ground. The voltage on the arm of 15 V ADJ potentiometer, R5, is fed to U1 where it is compared with the internal reference, referred to the ±15 V sense-return line, P103, pin 8. The current limit is imposed by sensing the drop across R9 and the circuit is stabilized by network R32,C7.

The regulated -15 V, 0.5A output at P103, pin 5, is established through Q2 and Q3 under the control of regulator amplifier U3-12. It uses the +15 V SENSE line as the reference, comparing it with the output through R10,R11 and the -15 V supply. Potentiometer R5, serves as the adjustment for both outputs. Current is limited by cutting the base drive to Q2 when the drop across R14 approaches one diode drop.

The regulated +5 V, 4 A output at P103, pins P and R, is established through Q4 and Q5 under the control of regulator U2 and a divider network, R18,R19. The +5 V SENSE line at P103, pins 13 and 14, is compared with the fraction of the U2 internal reference voltage appearing on the arm of 5 V ADJ potentiometer, R19. The current limit is imposed by sensing the drop across R24 through divider R22,R23. The circuit is stabilized by network R33,C12. The regulated -5 V, 0.5A output at P103, pin C, is established through Q6 and Q7 under the control of regulator amplifier U3-10. It uses the +5 V SENSE line as reference, comparing it with the output through R26,R27 and the -5 V SENSE line at P103, pin 3. The -5 V output tracks the +5 V supply and potentiometer R19 adjusts both. Output current is limited by cutting the base drive to Q6 when the drop across R30 approaches one diode drop.

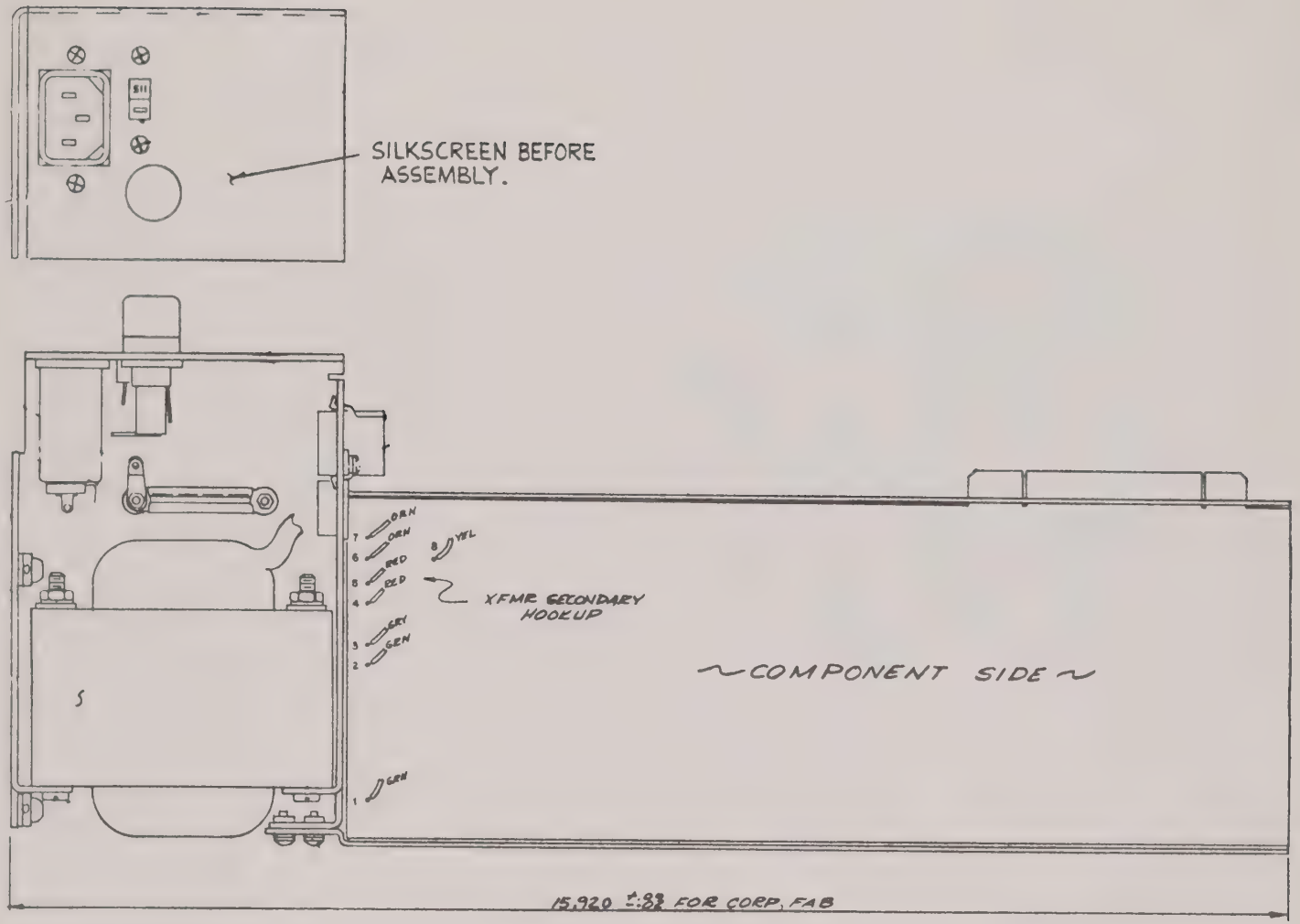


NOTES: (UNLESS OTHERWISE SPECIFIED)

1. COMPONENTS OUTSIDE DOTTED AREA ARE PART OF AC CHASSIS ASSY 41810-4-4.
2. ○ INDICATES NUMBERED PAD ON PC ASSY 41804-4-1.
3. □ INDICATES PIN NUMBER OF XA101 EDGE CONNECTOR ON PC ASSY 41804-4-1.
4. Ⓒ INDICATES TEST POINT.
5. ALL RESISTORS ARE IN OHMS, ¼W, 5%.
6. ALL CAPACITORS ABOVE 1µf ARE ALUM. ELECTROLYTIC, CAPACITORS BELOW 1µf ARE CERAMIC DISC.
7. ALL DIODES ARE IN4005.
8. U1 & U2 ARE µA723PC. U3 IS µA747PC.

POWER SUPPLY
SCHEMATIC #041810-7-9 REV B

8155-9-75

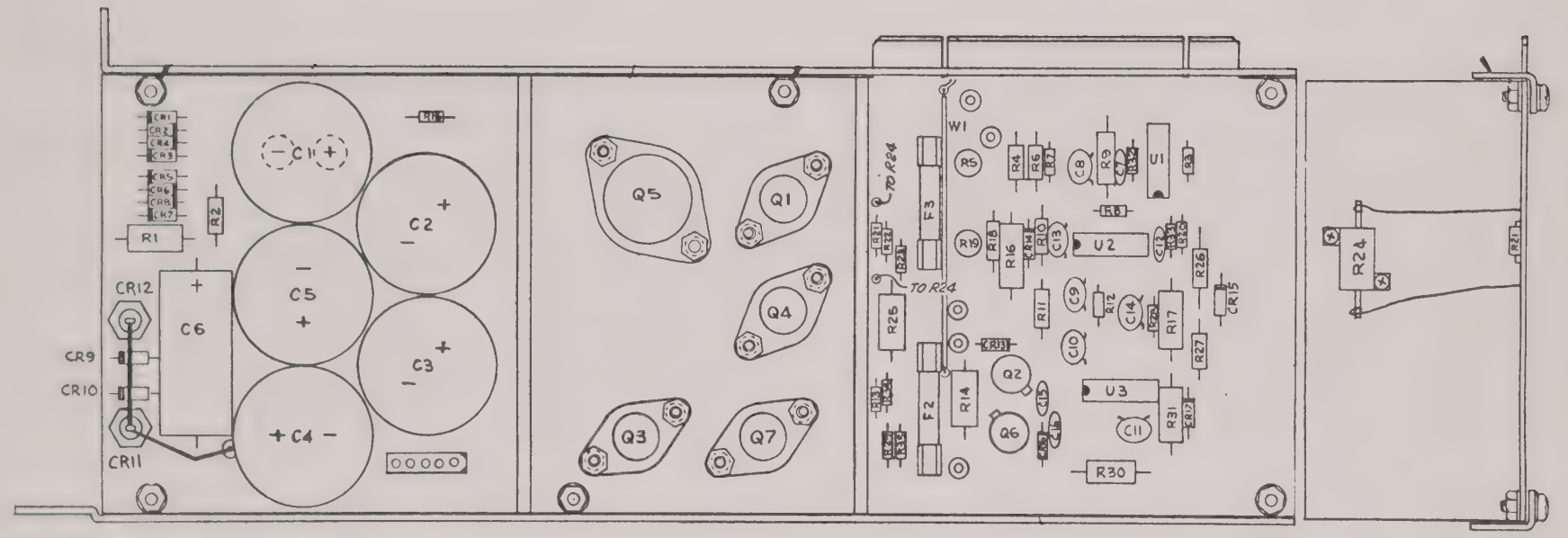


POWER SUPPLY ASSEMBLY #041810-4-9 REV A

PARTS LIST

POWER SUPPLY ASSEMBLY #041810-4-9 (REV A)

REF.	DESCRIPTION	SD PART NO.
	Assembly, Power Supply	041810-4-9
	Assembly, Power Supply Board	041804-4-9
	Schematic, Power Supply	041810-7-9
J101/Z1	Line Filter/Power Input	102461
XF1	Fuse, Post	102409
F1	Fuse, 2 A, Slo-Blo, 115 V	100585
S101	Switch, Slide 115/230 V, DPDT	102331
J102	Connector, 5 positive receptacle shell	101264
	Connector, Terminal, Female 18-24 ga.	10282201
T1	Transformer, Power	021408-6-1
	Strip, Terminal 4 point	100084 100084
	Cable, Power Supply	041810-3-6
	Chassis, AC	041810-1-6



POWER SUPPLY REGULATOR ASSEMBLY #041804-4-9 REV A

PARTS LIST

POWER SUPPLY BOARD #041804-4-9 (REV B)

REF.	DESCRIPTION	SD PART NO.
	Assembly	041804-4-9
	Schematic	041810-7-9
C1,2	Capacitor, 2700 µF 10%, 25 V	100232
C3,4	Capacitor, 13000 µF 10%, 15 V	116074
C5	Capacitor, 95 µF 10%, 350 V	100259
C6	Capacitor, 600 µF 10%, 15 V	100258
C7,12,15,16	Capacitor, 1000 pF 20%, 1 kV	100076
C8-11,13,14	Capacitor, .05 µF 20%, 50 V	100134
CR1-10,14,15,17	Diode, 1N4005	100413
CR11,12	Diode, MR1120R	100424
CR13,14	Diode, 1N4829	100443
F2	Fuse, 3 AG, 250 V	100592
F3	Fuse, 3 AG, 125 V	100584
J201	Connector, 5-positive Receptacle Shell	101264
Q1,3,4,7	Transistor, 2N3766	101373
Q2,6	Transistor, 2N2905	101382
Q5	Transistor, 40251	101354
R1	Resistor, 390 k 5%, 1 W, CC	101532
R2	Resistor, 220 k 5%, 1/2 W, CC	101458
R3,23	Resistor, 3.3 k 5%, 1/4 W, CC	101559
R4,6,18	Resistor, 4.7 k 5%, 1/2 W, CC	101511
R5,19	Potentiometer, 5 k 20%, 1/2 W	101859
R7,8,13,22,29	Resistor, 1 k 5%, 1/4 W, CC	101569
R9,14,30	Resistor, WW Power, .68 Ω 5%, 2 W	101829
R10,11,26,27	Resistor, 10 k 1%, .12 W Metal Film	101930
R12,28	Resistor, 4.7 k 5%, 1/4 W, CC	101598
R15,20	Resistor, 1.5 k 5%, 1/4 W, CC	101577
R16,17	Resistor, 1 k 5%, 1 W, CC	101635
R21	Resistor, 100 Ω 5%, 1/4 W, CC	101609
R24	Not Used	
R25	Resistor, 100 Ω 5%, 1 W, CC	101856
R31	Resistor, 330 Ω 5%, 1 W, CC	101624
R32,33	Resistor, 220 Ω 5%, 1/4 W, CC	101566
R34,35	Resistor, 39 Ω 5%, 1/4 W, CC	101733
U1,2	Integrated Circuit, 723PC	025761
U3	Integrated Circuit, 747PC	045205
XF1	Not Used	
XF2,3	Socket, Fuse	102745

PARTS LIST

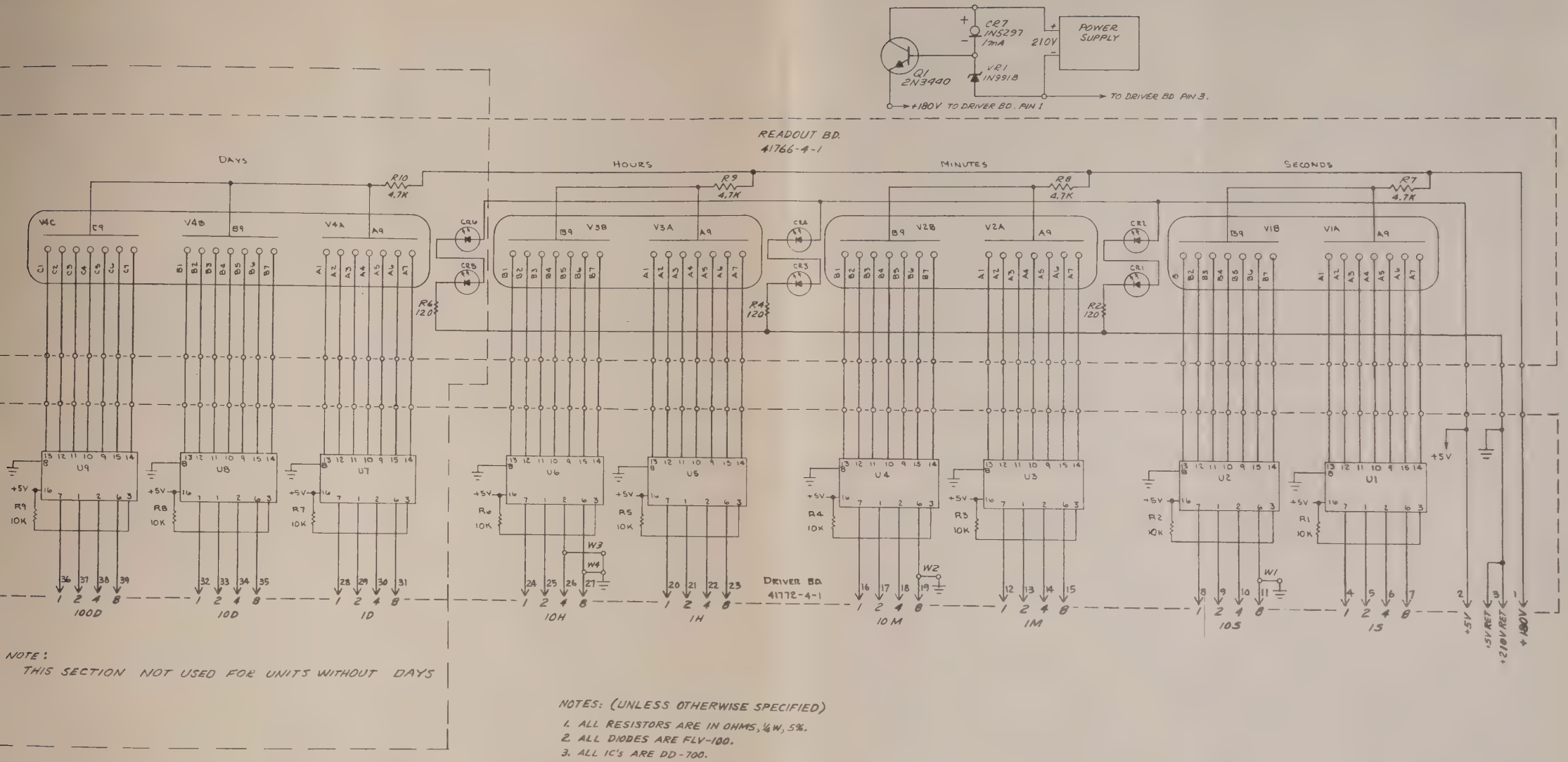
POWER SUPPLY BOARD #041804-4-9 (Cont'd)

REF.	DESCRIPTION	SD PART NO.
XQ1,3-5,7	Connector, Pin Socket	102442
XU1-3	Socket, 14-pin	102483
	Test Point, Red	100541
	Test Point, Black	100542
	Test Point, Green	100543
	Test Point, Blue	100547
	Test Point, Violet	100548
	Insulator, 7-pin	03946604
	Socket, Connector	103037
	Connector, PC Male	10282203
	Angle, Front	041811-1-2
	Angle, Rear	041812-1-2

CIRCUIT DESCRIPTION
DISPLAY ASSEMBLY
SCHEMATIC #041945-7-2

1) GENERAL

The basic display assembly has three 2-digit, in-line, planar indicator tubes and associated driver chips for the display of time in hours, minutes and seconds. LED colons are provided between the tubes. The assembly includes provision for the addition of a 3-digit days display plus a third colon when the Days Option is included. Time information is accepted in parallel BCD form.

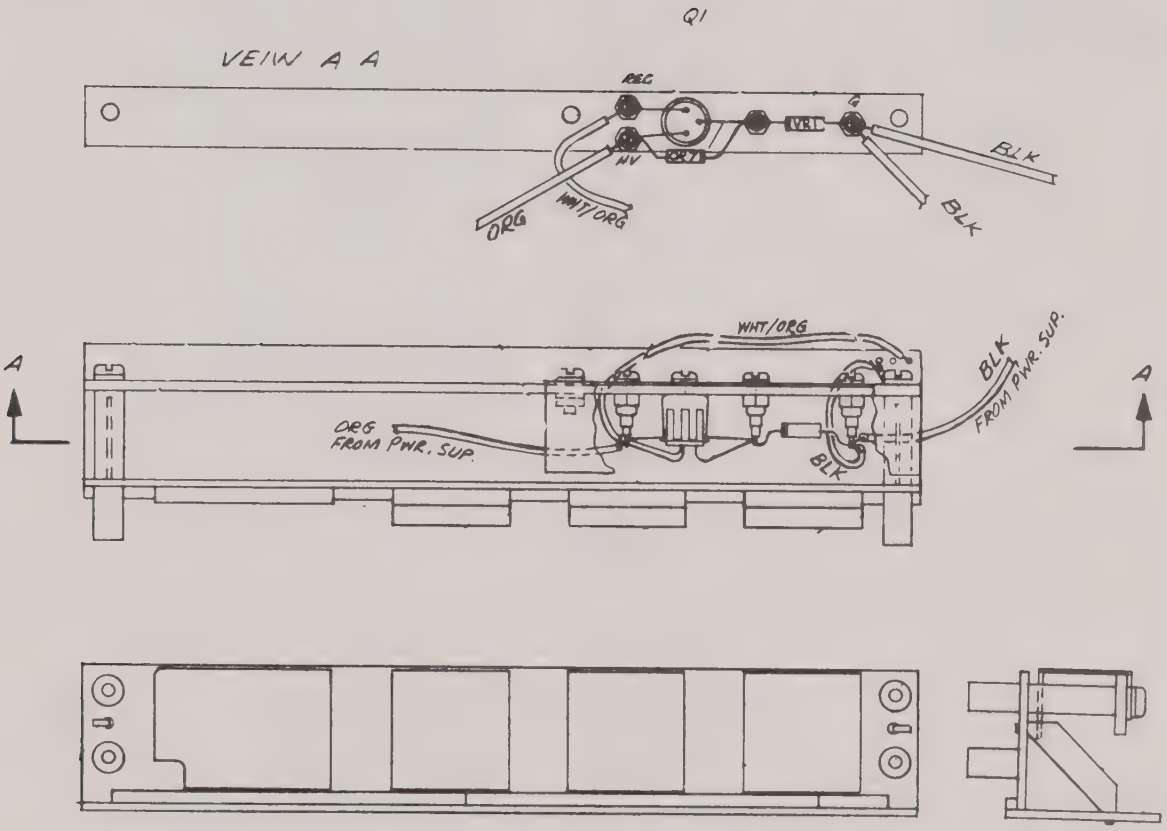


NOTE:
THIS SECTION NOT USED FOR UNITS WITHOUT DAYS

NOTES: (UNLESS OTHERWISE SPECIFIED)

1. ALL RESISTORS ARE IN OHMS, ¼W, 5%.
2. ALL DIODES ARE FLV-180.
3. ALL IC'S ARE DD-700.

READOUT & DRIVER
SCHEMATIC #041945-7-2 REV F

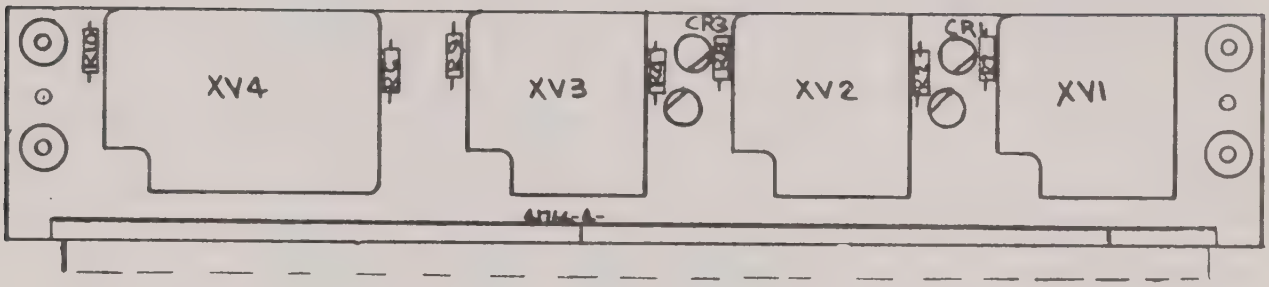


DISPLAY ASSEMBLY, 6-DIGIT #041945-4-2 REV D

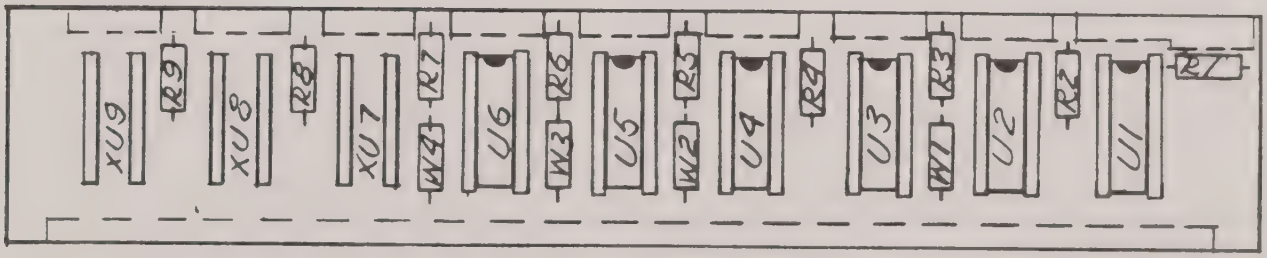
PARTS LIST

DISPLAY ASSEMBLY, 6-DIGIT #041945-4-2 (REV E)

REF.	DESCRIPTION	SD PART NO.
	Assembly, Display & Driver	041945-4-2
	Assembly, Display	041766-4-1
	Assembly, Driver	041772-4-1
	Schematic	041945-7-2
CR7	Diode, 1N5297	100457
Q1	Transistor, 2N3440	101420
V1-3	Tube, Display SP352 Sperry	102403
VR1	Diode, 1N991B	100461
	Bracket, Display & Driver Board	051450
	Bracket	06197402
	Insulator	061977
	Heatsink	103079



DISPLAY ASSEMBLY, 9-DIGIT #041766-4-1 REV G



DRIVER ASSEMBLY, 9-DIGIT #041772-4-1 REV D_1

PARTS LIST

DISPLAY ASSEMBLY #041766-4-1 (REV F)

REF.	DESCRIPTION	SD PART NO.
	Assembly	041766-4-1
	Schematic	041945-7-2
CR1-4	Lamp, LED	100455
R2,4,6	Resistor, 120 Ω 5%, 1/4 W, CC	101717
R7-10	Resistor, 4.7 k 5%, 1/4 W, CC	101598
XV1-3	Socket, 2-Digit Display	102445
XV4	Socket, 3-Digit Display	102446
	Connector, 30-pin Right Angle Male	101277
	Connector, 6-pin Right Angle	051451

DRIVER ASSEMBLY #041772-4-1 (REV E)

REF.	DESCRIPTION	SD PART NO.
	Assembly	041772-4-1
	Schematic	041945-7-2
R1-9	Resistor, 10 k 5%, 1/4 W	101570
U1-6	Integrated Circuit, Sperry DD700	045203
W1-4	Jumper, Molded	102879
	Socket, 16-pin Dip	103350

CHAPTER 6
STANDARD OPTION

6.1 GENERAL

Several standard options are available for the Model 8155. When supplied with the instrument, all options will be described on the following pages.

CIRCUIT DESCRIPTION
IRIG A OUTPUT (OPTION C11Q)
SCHEMATIC #05189607

1) GENERAL

The IRIG A Output option adds Dwg. #021554-7-1 Code Generator (A17), #021556-7-3 Shaper Modulator (A22), BNC connectors (J7 and J8) and associated wiring to the basic unit.

2) SPECIFICATIONS

MODULATED CODE: The modulated code is generated on a 10 kHz carrier with an adjustable amplitude for 0 to 10 V peak-to-peak from a low impedance 15 mA source and an adjustable modulation ratio (Mark-to-Space) from 2:1 to 6:1. Connector is rear panel BNC type. The Code Format is modified IRIG A with BCD hours, minutes, seconds and tenths of seconds. (Days are included if Option E20 is installed.)

DC LEVEL SHIFT CODE: The DC Level Shift code is generated with an ad-us justable amplitude from 0 to 10 V into a minimum 600 Ω load. Connector is rear panel BNC type. Both outputs are short-circuit proof to ground.

3) SHAPER/MODULATOR ADJUSTMENTS Dwg. #021556-7-3

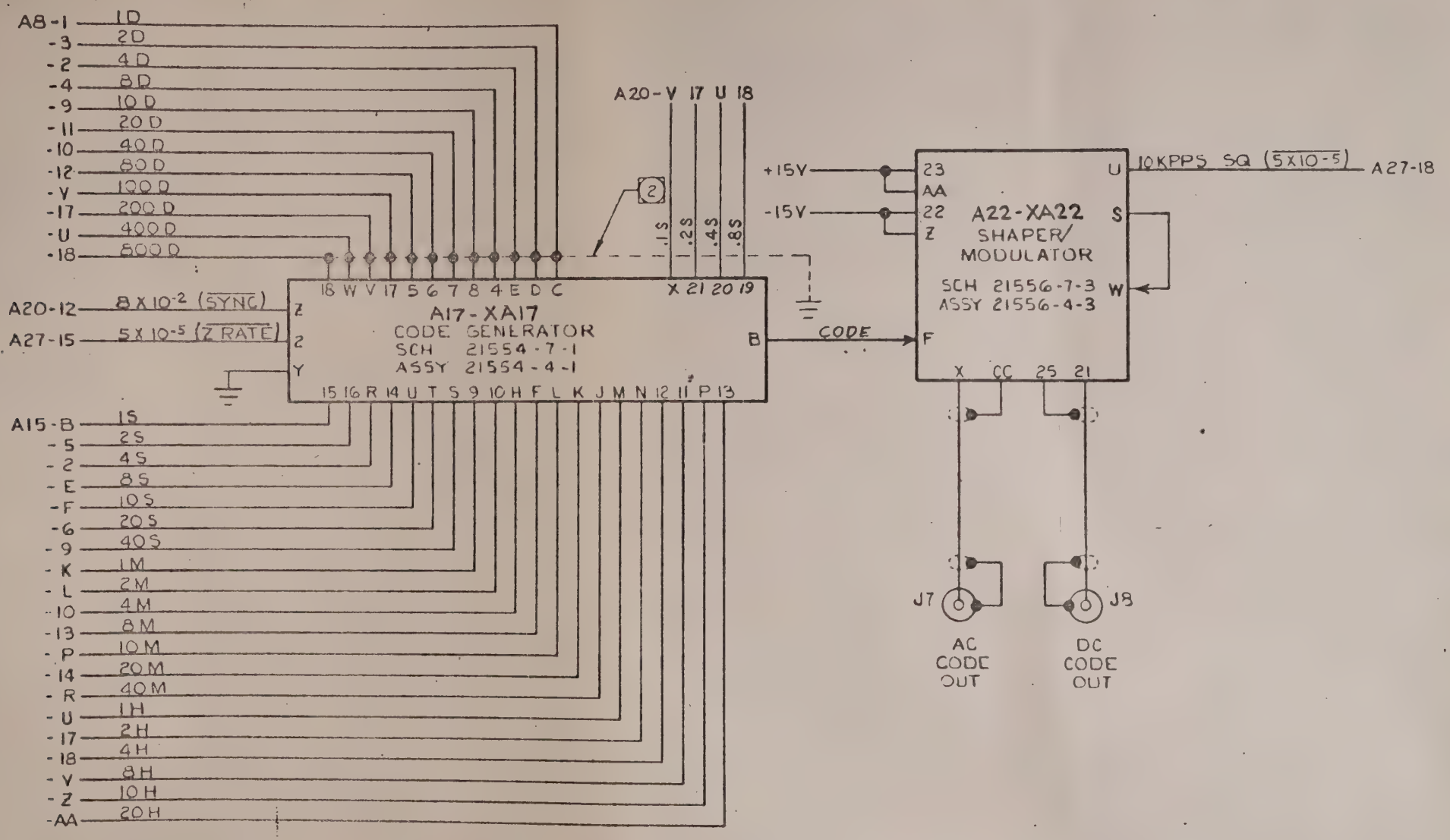
a) Adjust TUNE R43(-4)/R53(-5) control for maximum AC signal at the MOD test point.

b) Adjust MOD R20 control for a nominal 3 V peak-to-peak output of the Large Cycle signal.

c) Adjust RATIO R16 control for a 3:1 modulation ratio.

d) Return to the TUNE R43(-4)/R53(-5) control and adjust until the junction point of the large and small cycles has a minimum of distortion.

e) Adjust DC Code R23 amplitude control for a nominal output of 3 V peak-to-peak.



] CONNECT LEADS SHOWN TO A8 FOR E20; WITHOUT E20 OPTION, CONNECT THE PINS OF A17 TO GND.

. THE CIRCUITRY SHOWN IS SUPERIMPOSED ON BASIC BLOCK DIAGRAM 51206-7-1.

NOTES:

PROPRIETARY DATA

SYSTRON DONNER CORPORATION
CONCORD CALIFORNIA
CODE IDENT 53947

IRIG A OUTPUT CIIQ OPTION

8155

7

05189607 A

PARTS LIST

IRIG A OUTPUT (C11Q OPTION) #05189607 REV A

REF.	DESCRIPTION	SD PART NO.
	ADD	
	Schematic	05189607
A17	Assembly, Code Generator	021554-4-1
A22	Assembly, Shaper/Modulator	021556-4-3
J7,8	Connector, BNC	101155
XA17,22	Connector, P.C. Edge	101204
	Insulator, BNC	100823
	Washer, Fiber	101074
	DELETE	
J7,8	Hole Plug, BNC	100952

CIRCUIT DESCRIPTION
SHAPER/MODULATOR
SCHEMATIC #21556-7-3

1) GENERAL

The Shaper/Modulator card can be assembled to provide up to three shaper circuits, a modulator, a dc code output buffer, a Days/ID control circuit, a square wave decoder and miscellaneous inverters and buffers. The shaper circuits are identical with the exception that three capacitors within each circuit are a function of frequency. The following description is intended to apply to all card configurations. The specific assembly used is covered by the attached assembly, schematic and parts list.

2) SHAPERS

Each of the shaper circuits (up to three) are identical, with the exception that the values chosen for three capacitors in each circuit are inversely proportional to the resonant frequency. Each shaper accepts a logic level square wave at the selected carrier frequency and outputs an in-phase sine wave which may be selected (through switching external to the card) and fed to the modulator. The input is filtered and applied to the base of a constant-current amplifier which drives an active circuit having the electrical properties of a tuned tank circuit. A potentiometer is provided to adjust the resonant frequency. The sine wave output from this circuit is buffered and ac-coupled to output pin M, S or T.

3) MODULATOR

The modulator accepts the selected carrier sine wave at pin W and modulates it with the dc level shift code at pin F. The resulting modulated code is fed through amplifier A4 to output pin X.

A MODULATION RATIO adjustment, R16, sets the percentage of modulation before the signal is fed to A4. A MODULATED CODE AMPLITUDE adjustment, R20, determines the gain of amplifier A4, thus, establishing the signal level at pin X. (0 to ±10 V p-p.)

4) DC CODE BUFFER

The dc level shift code input to pin F is inverted once by A1-11 and again by Q4 before being fed as the dc code output to pin 21, through R25. Transistors Q2 and Q3, and the DC CODE AMPLITUDE potentiometer R23, establish the output level at pin 21 (0.4 V to +10 V). Short-circuit protection is provided by CR3, CR4 and R24. The quiescent current in Q3 and Q4 is determined by CR3, CR5 and R25.

5) DAYS/ID (RUN NUMBER) CONTROL

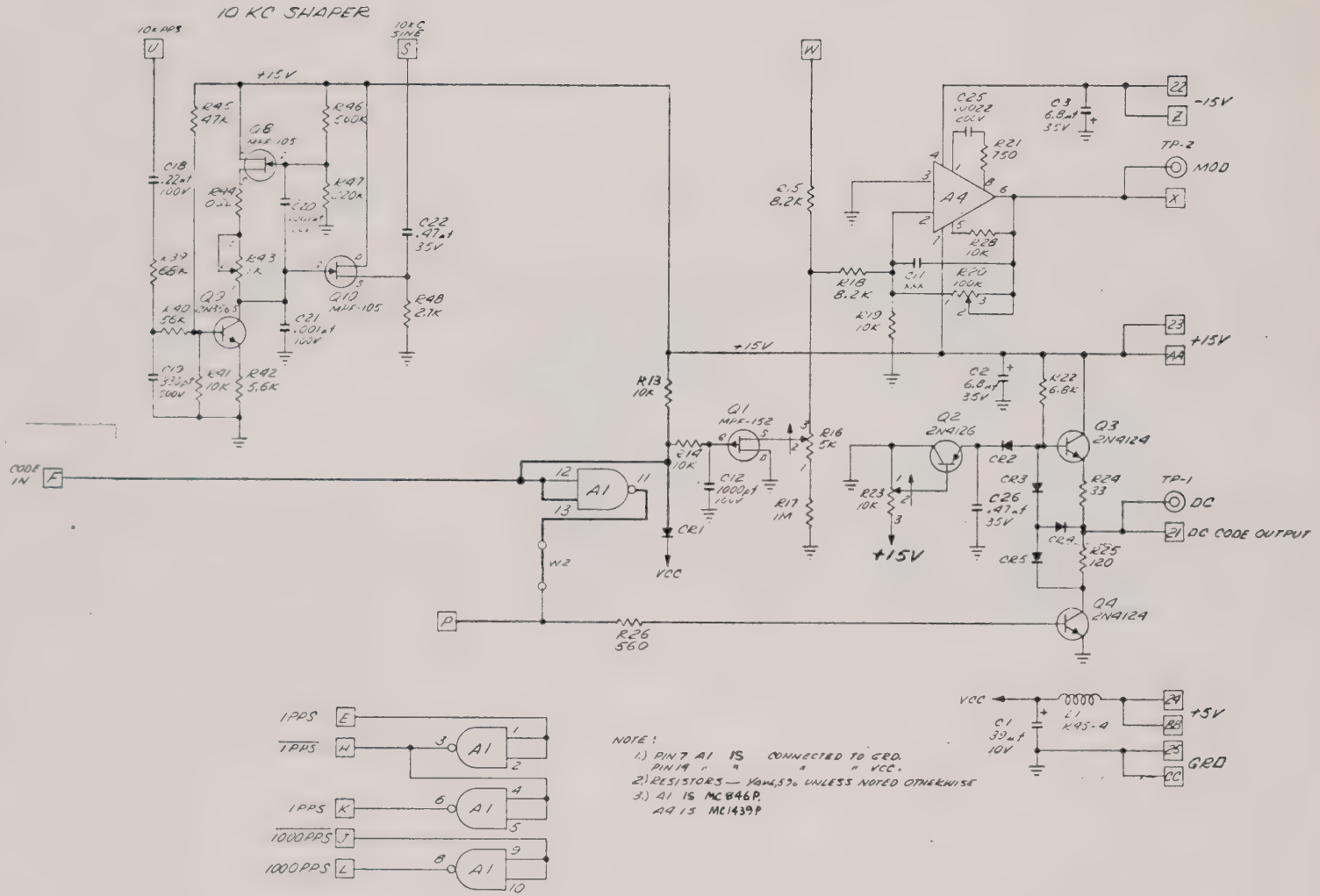
Gates on A3 control the selection of the signal which is used to update the days accumulator in the system. The carry output from the time-of-day accumulator is inverted and applied to A3-9. If the other input (the $\overline{\text{ID NUM}}$ line) is high (i.e. left open), the hours accumulator carry will update the days accumulator. Similarly, a high on the $\overline{\text{DAYS}}$ line permits a signal on pin B ($\overline{\text{ID NUM ADV}}$) to update the days accumulator. The ID advance input pulses are standardized by one-shot A3-3,6 to ensure reliable operation.

6) SQUARE WAVE DECODER

This circuit, formed from gates on A2, generates a square wave from the BCD outputs fed to pins C, D and N from an external decade counter. It consists of a flip-flop (A2-8,11) which is ac-set at mid-period when the output from A2-6 goes to ground ("1" and "4" bits both positive). The flip-flop is ac-reset by the trailing edge of the "8" bit. The result is a square wave at A2-11. The output pulse rate is a function of the source of input signals.

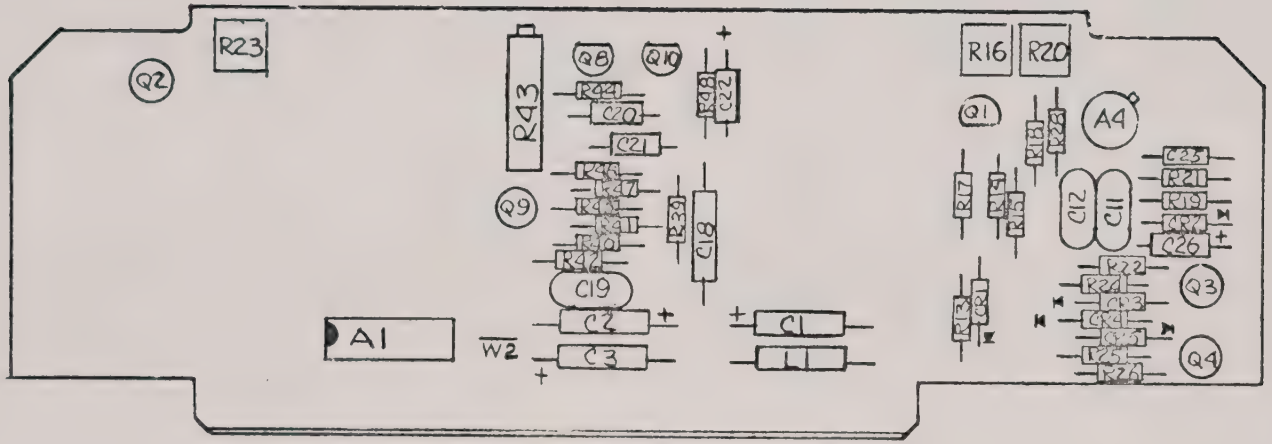
7) BUFFERS

Extra gates on A1 and A2 are made available for external use as inverters and buffers.



NOTE:
1.) PIN 7 A1 IS CONNECTED TO GRD.
PIN 14 " " " " VCC.
2.) RESISTORS — Y&W, 5% UNLESS NOTED OTHERWISE
3.) A1 IS MC846P.
A4 IS MC1439P

SHAPER/MODULATOR SCHEMATIC #21556-7-3



SHAPER/MODULATOR ASSEMBLY #21556-4-3 REV A

PARTS LIST

SHAPER & MODULATOR #021556-7-3

REF.	DESCRIPTION	SD PART NO.
	Assembly	021556-4-3
	Schematic	021556-7-3
A1,3	Integrated Circuit, MC846P	019716
A4	Integrated Circuit, MC1439G	025729
C1	Capacitor, 39 µF, 10 V	100183
C2,3	Capacitor, 6.8 µF, 35 V	100182
C11	Capacitor, Factory Selected	XXXXXX
C12	Capacitor, 1000 pF, 100 V	100243
C18	Capacitor, .22 µF, 100 V	100148
C19	Capacitor, 330 pF, 500 V	100276
C20,21	Capacitor, .001 µF, 100 V	100137
C22,26	Capacitor, .47 µF, 35 V	100140
C25	Capacitor, .0022 µF, 200 V	100185
CR1-5	Diode, 1N4151	100385
L1	Inductor, R45-4	101313
Q1	Transistor, MPF-152	101383
Q2	Transistor, 2N3906	101378
Q3,4	Transistor, 2N3904	101377
Q8,10	Transistor, MPF-105	101384
Q9	Transistor, 2N3565	101371
R13,14,19,28, 41	Resistor, 10 k, 1/4 W, 5%, CC	101570
R15,18	Resistor, 8.2 k, 1/4 W, 5%, CC	101595
R16	Resistor, 5 k, 62 PA, Var.	101845
R17	Resistor, 1 M, 1/4 W, 5%, CC	101605
R20	Resistor, 100 k, 62 PA, Var.	101934
R21	Resistor, 750 Ω, 1/4 W, 5%, CC	101689
R22	Resistor, 6.8 k, 1/4 W, 5%, CC	101544
R23	Resistor, 10 k, 62 PA, Var.	101937
R24	Resistor, 18 Ω, 1/4 W, 5%, CC	101727
R25	Resistor, 120 Ω, 1/4 W, 5%, CC	101717
R26	Resistor, 560 Ω, 1/4 W, 5%, CC	101583
R39	Resistor, 68 k, 1/4 W, 5%, CC	101597
R40	Resistor, 56 k, 1/4 W, 5%, CC	101670
R42	Resistor, 5.6 k, 1/4 W, 5%, CC	101584
R43	Resistor, 1 k, Beckman, 79 P, Var.	101181

PARTS LIST

SHAPER & MODULATOR #021556-7-3 (Cont'd)

REF.	DESCRIPTION	SD PART NO.
R45	Resistor, 47 k, 1/4 W, 5%, CC	101574
R46	Resistor, 560 k, 1/4 W, 5%, CC	101687
R47	Resistor, 220 k, 1/4 W, 5%, CC	101610
R48	Resistor, 2.7 k, 1/4 W, 5%, CC	101599
	Extractor	100867

CIRCUIT DESCRIPTION
CODE GENERATOR
SCHEMATIC #21554-7-1

1) GENERAL

The IRIG DC Code Generator card can be used to generate the IRIG A,B, C,E or H codes. Code selection may be remotely controlled or fixed by the particular card configuration. Days information may be optionally included and provision is made for the insertion of control function bits and/or straight binary seconds from a source external to the card. The following description is intended to apply in general to all configurations of the card. The specific assembly used is identified by the attached assembly, schematic and parts list.

2) DIVIDER CIRCUITS

Refer to the timing diagrams and the schematic for this and subsequent sections. Divider A8 is a divide-by-two, then-by-five counter which divides down the "Z RATE" and provides decoded outputs for the code generating gates. Divider A15 is a divide-by-five, then-by-two counter which takes the output of A8 divides it down and supplies decoded outputs for the scan gates and the code generating gates. Divider A17 is a divide-by-two, then-by-six counter. Its principle function is to control the secondary scan gate A4. The divide-by-twelve is used only for IRIG C, the divider being reset at the count of ten or by the sync input for the other codes. This early reset is shown on the timing diagram as A18-8. The reset pulse is quite short and therefore has been widened for clarity. The area between the dotted lines on Sheet 2 is simply eliminated when the divider resets at ten. Reset at ten is established by gate A18-8. A one-shot (A18-12,6) performs code frame reset. The external reset signal (pin Z) may be used for code frame reset when W1 is installed, or the card can supply a reset to synchronize the associated accumulator when W2 is installed.

Divider A7 (if present) is a divide-by-five counter provided for external use. It is synchronized with the other divider chips.

3) SCAN GATES

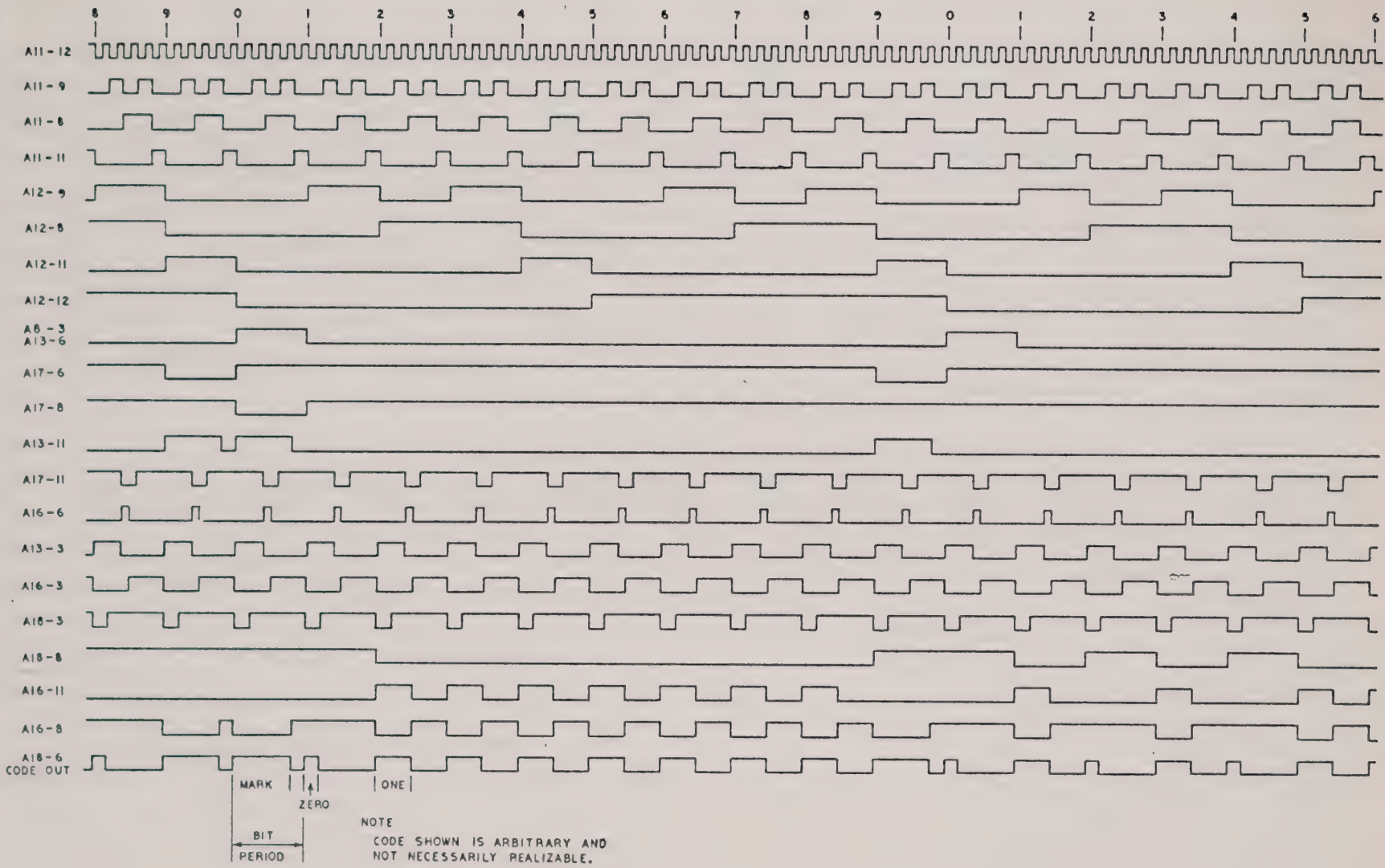
Creation of serial ONES is accomplished by a two-stage switching network and a series of gates. Chips A10-A14 are basically single pole (pin 8 is the output), 8-position switches. The inputs to these switches are the time data from the system accumulator. (One or more of these chips may be deleted on a particular card configuration.) The switching is controlled by BCD information on pins 1, 2 and 13. Since the above switches have the BCD inputs in parallel, all the time decades will provide outputs simultaneously; thus, the need for switch A4. This switch, controlled from the BCD outputs of divider A17, selects the proper time interval for serializing each switch output. (The series of gates associated with A14 and A13, if present, further control these switches which may have outputs that should not be

present in certain codes.) For example, tenths-of-seconds are added only in IRIG A, units-of-seconds are deleted in IRIG E, and all seconds information is deleted in IRIG C. Gates A5-8, A5-11 and A3-8 are used to inhibit the presence of serials ONES at certain times when no serial ONES should be present. This prevents the spurious ONES (coming from the switches) from appearing in the output code.

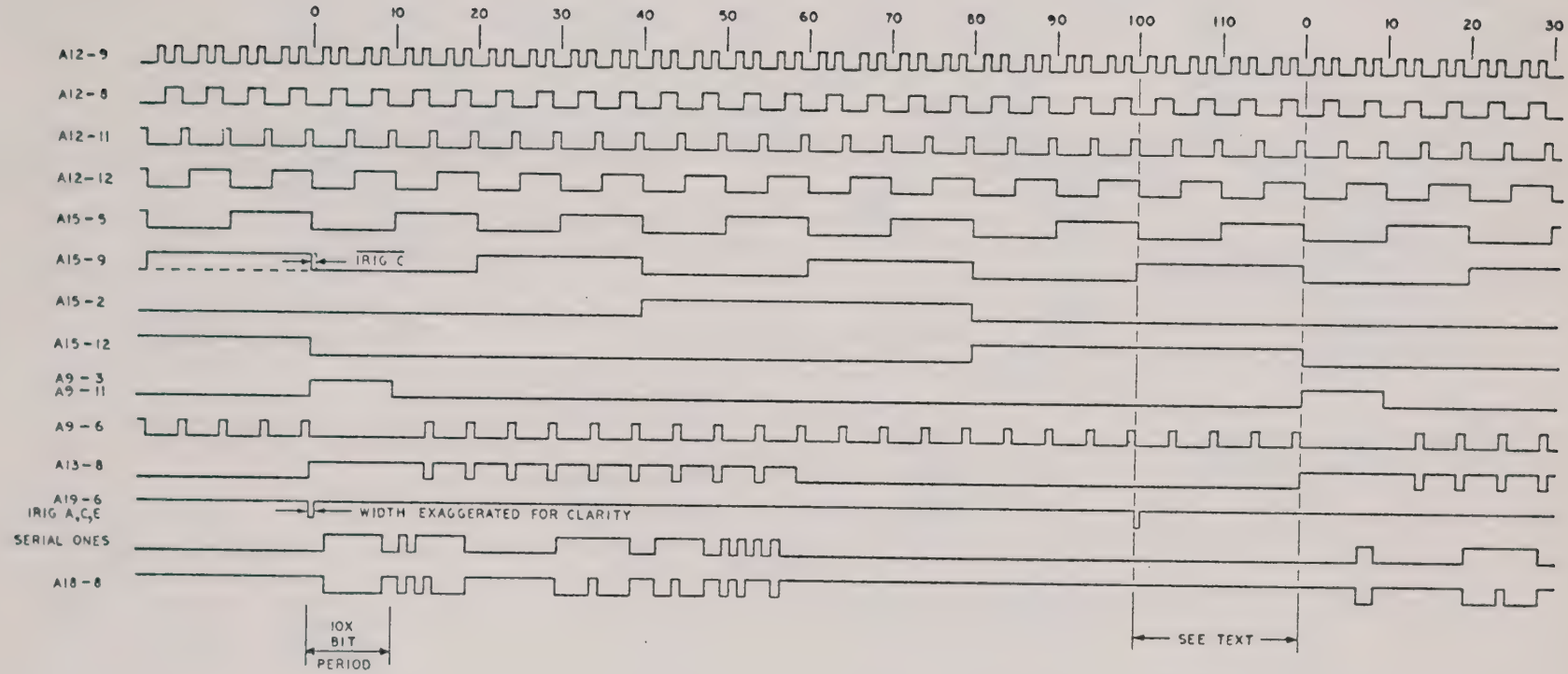
4) CODE GENERATING GATES

These gates must generate three time intervals in a 2:5:8 ratio. The time for the intervals is dependent on the bit period and is determined by the "Z RATE" on pin 2. A "2" length is a ZERO, a "5" is a ONE, and an "8" is an INDEX MARKER.

The INDEX MARKERS are generated by gating the output of divider A15. Gate A1-3 adds information from the output of divider A11 to create the "8" width. Gates A6-8 and A6-11 allow an extra pulse from gates A2-6 and A2-8 to give the "double-mark" at the start of the frame. Gate A3-6 provides the marker at each tenth frame interval. Gate A9-11 supplies a pulse of "2" width at the start of each bit interval. If a MARKER or a ONE is not present, then the output code will be high for only the "2" width. Gate A1-6 supplies the "5" width pulse. This is AND-gated with the SERIAL ONES from A3-8 by gate A1-8. (External bits may be inserted on this same line through pin 22.) The presence of a ONE will cause the "5" width to appear in the output code, masking the "2" width which is always present. Gates A2-3 and A9-8 are used to combine the various widths to produce the output code at pin B.

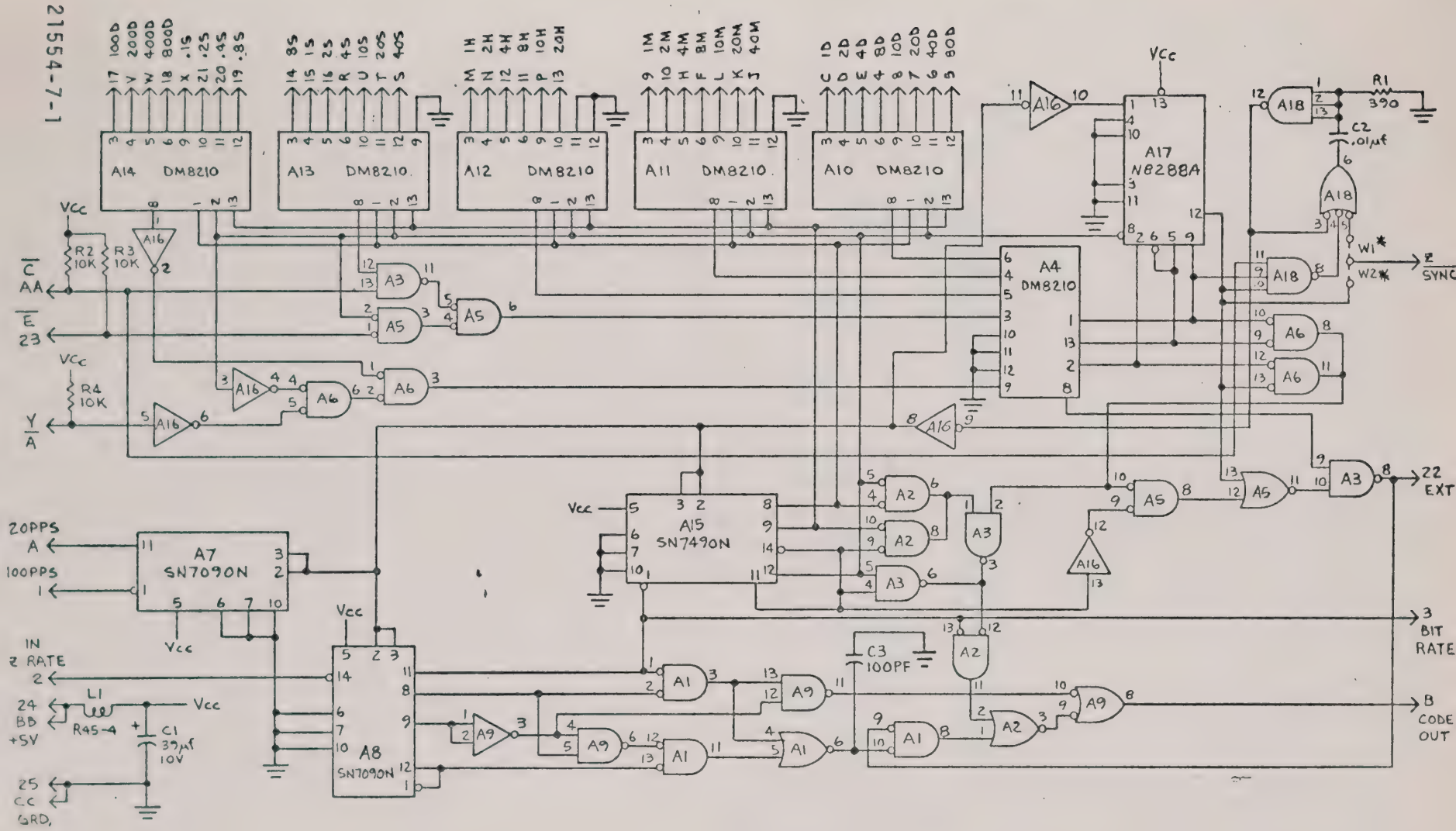


IRIG DC CODE GENERATOR - TIMING DIAGRAM - (Sheet 1 of 2)

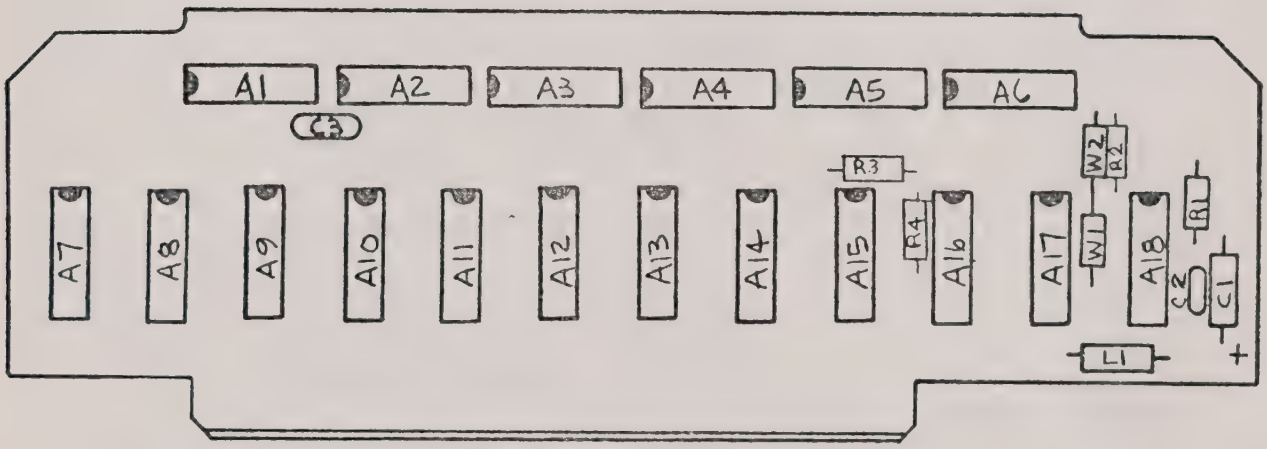


NOTE:
CODE SHOWN (SERIAL ONES & A18-8) IS ARBITRARY AND NOT NECESSARILY REALIZABLE.

IRIG DC CODE GENERATOR - TIMING DIAGRAM - (Sheet 2 of 2)



SWITCHABLE GENERATOR IRIG A-B-C-E SCHEMATIC #B21554-7-1D



CODE GENERATOR ASSEMBLY #021554-4-1 REV C

PARTS LIST

CODE GENERATOR ASSEMBLY #021554-4-1

REF.	DESCRIPTION	SD PART NO.
	Assembly	021554-4-1
	Schematic	021554-7-1
A1,2,5,6	Integrated Circuit, MC1810P	025735
A3,9	Integrated Circuit, MC846P	019716
A4,10-14	Integrated Circuit, DN8210	025746
A7,8,15	Integrated Circuit, SN7090N	025732
A16	Integrated Circuit, MC836P	025704
A17	Integrated Circuit, N8288A	025723
A18	Integrated Circuit, SN7410N	019706
C1	Capacitor, 39 µF, 10 V	100183
C2	Capacitor, .01 µF, 100 V	100103
C3	Capacitor, 100 pF, 500 V	100173
L1	Inductor, R45-4	101313
R1	Resistor, 390 Ω 5%, 1/4 W	101592
R2-4	Resistor, 10 k 5%, 1/4 W	101570
	Jumper, Molded	102879
	Extractor	100865

CIRCUIT DESCRIPTION
IRIG B OUTPUT (OPTION C12Q)
SCHEMATIC #7-05189601/08

1) GENERAL

The IRIG B Output option adds Dwg. #21554-7-1 Code Generator (A13), #21556-7-5 Shaper Modulator (A24), BNC connectors (J5 and J6) and associated wiring to the basic unit.

2) SPECIFICATIONS

MODULATED CODE: The Modulated Code is generated on a 1 kHz carrier with an adjustable amplitude for 0 to 10 V peak-to-peak from a low impedance 15 mA source and an adjustable modulation ratio (Mark-to-Space) from 2:1 to 6:1. Connector is rear panel BNC type. The Code Format is modified IRIG B with BCD hours, minutes and seconds. (Days are included if Option E20 is installed.)

DC LEVEL SHIFT CODE: The DC Level Shift Code is generated with an adjustable amplitude from 0 to 10 V into a minimum 600 Ω load. Connector is rear panel BNC type. Both outputs are short-circuit proof to ground.

3) SHAPER/MODULATOR ADJUSTMENTS Dwg. #21556-7-5

a) Adjust TUNE R43(-4)/R53(-5) control for maximum ac signal at the MOD test point.

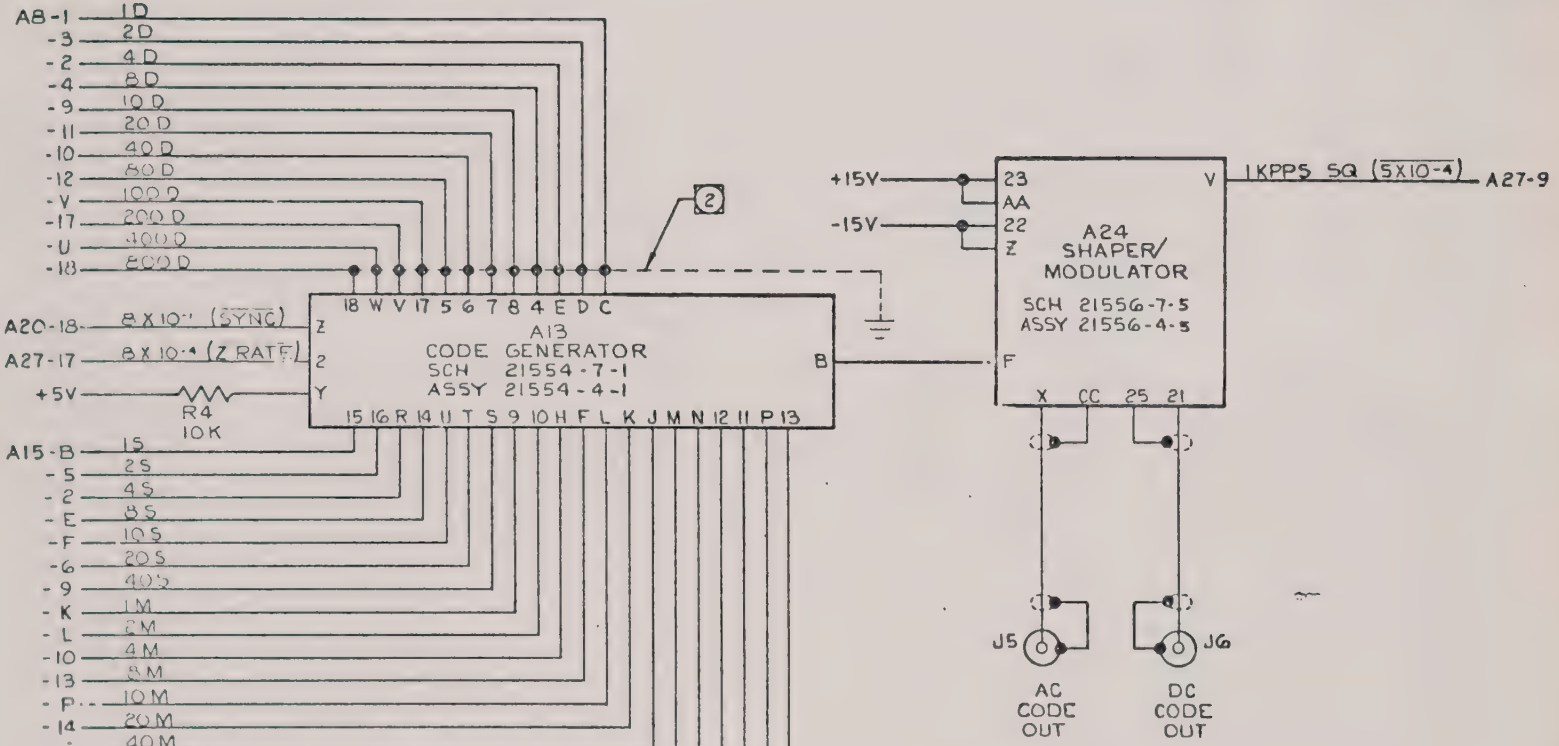
b) Adjust MOD R20 control for a nominal 3 V peak-to-peak output of the Large Cycle signal.

c) Adjust RATIO R16 control for a 3:1 modulation ratio.

d) Return to the TUNE R43(-4)/R53(-5) control and adjust until the junction point of the large and small cycles has a minimum of distortion.

e) Adjust DC Code R23 amplitude control for a nominal output of 3 V peak-to-peak.

REVISIONS					
LTR	DESCRIPTION	ENG ORD NO	DATE	ENG	APP
A	REMOVED DWG No. IN NOTE 1	—	11/1/		
B	A24 WAS 21556-7-2 & 21556-4-2		11/04		



(2) CONNECT LEADS SHOWN TO A8 FOR E20; WITHOUT E20 OPTION, CONNECT THE PINS OF A13 TO GND.

1. THE CIRCUITRY SHOWN IS SUPERIMPOSED ON BASIC BLOCK DIAGRAM.

NOTES:

PROPRIETARY DATA

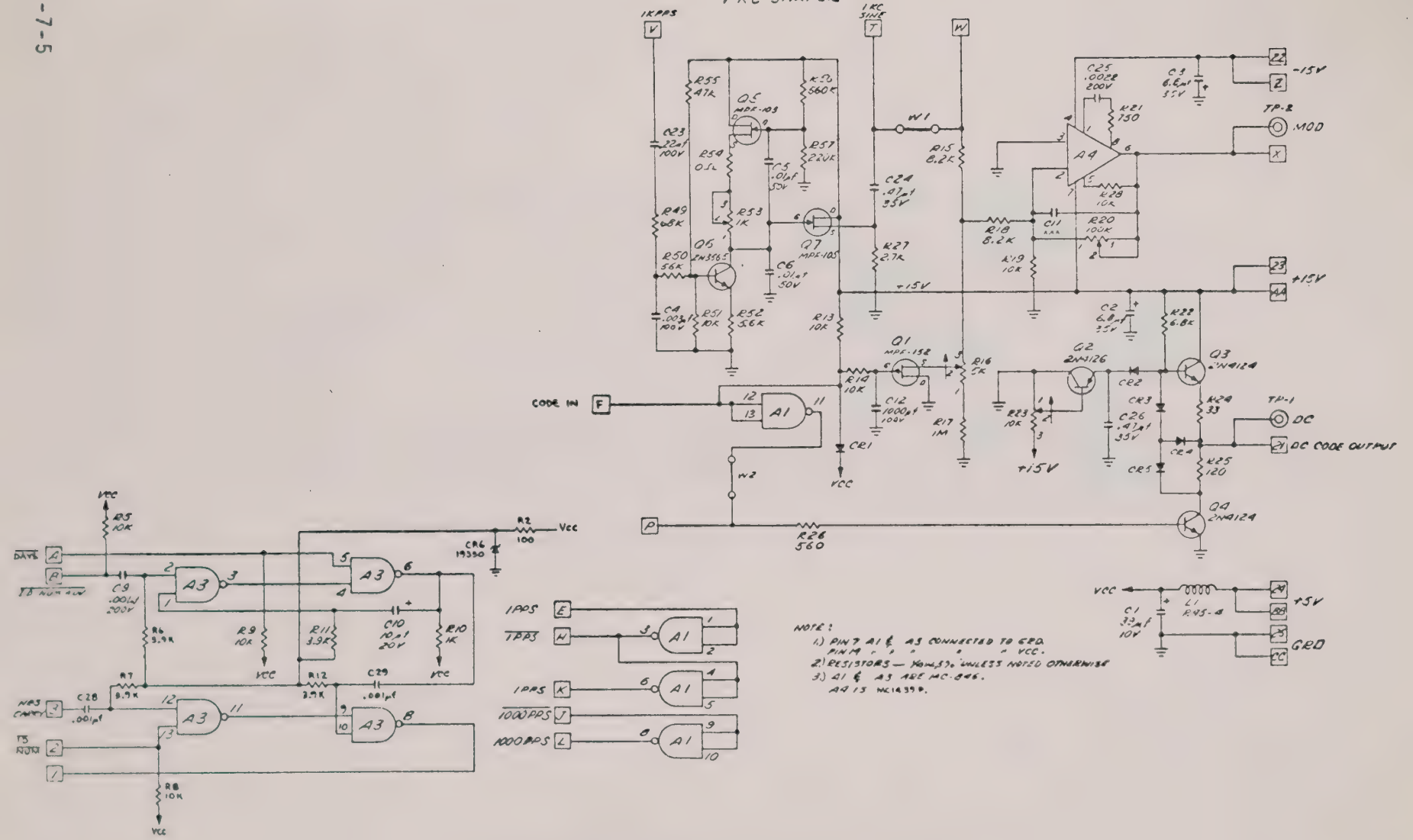
Furnished under United States Government Contract No. ... Such data may be either released outside the Government, or used, duplicated or disclosed in whole or in part for manufacture or procurement, without the written permission of System Develop. Corporation, except for: (1) other parts of objects or proprietary stock by or for the Government where the need to procure such items or data pertaining to them is evident at the time of or in connection with the delivery of the items furnished to the Government; or (2) emergency overhaul or repair work by or for employees of the United States Government, when the essential purpose of such overhaul or repair cannot be accomplished unless such data is used for manufacture; provided that in either case this notice shall be affixed to any such data disclosed, and that with respect to data identified as being proprietary data, it is disclosed only for the purposes stated above.

		DRAWN	DATE	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	SYSTEM DEVELOPMENT CORPORATION CONCORD CALIFORNIA	IRIG B OUTPUT C12Q OPTION	
		CHECK	DATE				
		ENGR	DATE				
		PROJECT	DATE				
		Q A	DATE		CODE IDENT 06811		
8155A							
USED ON	NEXT ASSY	MATERIAL			SIZE 7	21556-01	REV B
APPLICATION		DO NOT SCALE DRAWING		SHEET 1			

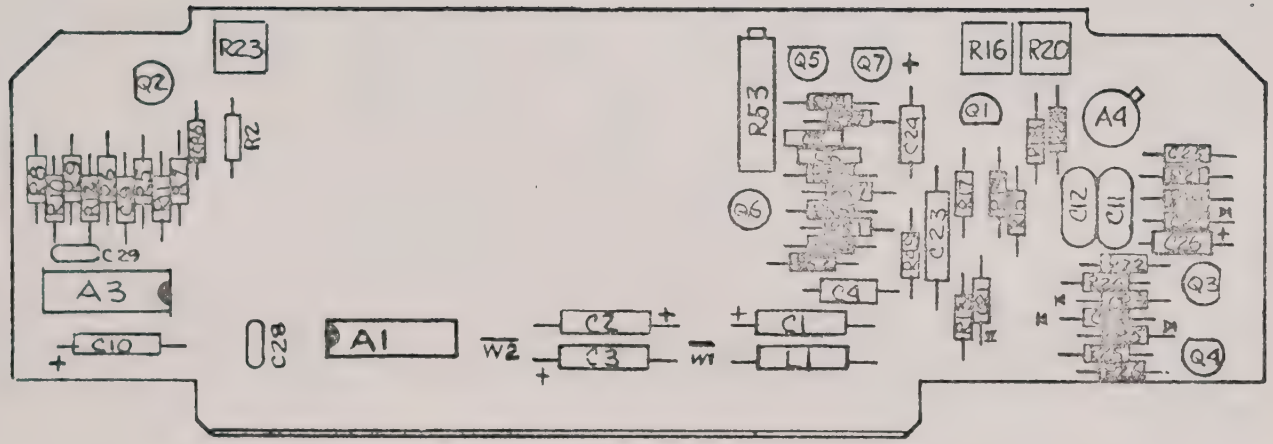
PARTS LIST

OPTION C12Q IRIG B OUTPUT #7-05189601

REF.	DESCRIPTION	SD PART NO.
	ADD	
	Schematic	7-05189601
A1-12	Not Used	
A13	Assembly, Code Generator	021554-4-1
A14-23	Not Used	
A24	Assembly, Shaper/Modulator	021556-4-5
J1-4	Not Used	
J5,6	Connector, BNC	101155
R1-3	Not Used	
R4	Resistor, 10 k 5%, 1/4 W	101570
XA1-12	Not Used	
XA13	Connector, Edge	101204
XA14-23	Not Used	
XA24	Connector, Edge	101204
	DELETE	
J5,6	Plug, Hole BNC	100952



MODULATOR SCHEMATIC #21556-7-5 REV B



SHAPER & MODULATOR ASSEMBLY #B21556-4-5B

PARTS LIST

SHAPER & MODULATOR #021556-7-5

REF.	DESCRIPTION	SD PART NO.
	Assembly	021556-4-5
	Schematic	021556-7-5
A1-3	Integrated Circuit, MC846P	019710
A4	Integrated Circuit, MC1439G	025729
C1	Capacitor, 39 µF, 10 V	100183
C2,3	Capacitor, 6.8 µF, 35 V	100182
C4	Capacitor, .0033 µF, 200 V	100153
C5,6	Capacitor, .01 µF, 50 V	100132
C9	Capacitor, .001 µF, 200 V	100137
C10	Capacitor, 10 µF, 20 V	100063
C11	Capacitor, Factory Selected	XXXXXX
C12	Capacitor, 1000 pF, 100 V	100243
C23	Capacitor, .22 µF, 100 V	100148
C24,26	Capacitor, .47 µF, 35 V	100140
C25	Capacitor, .0022 µF, 200 V	100185
C28,29	Capacitor, .001 µF, Disc	100076
CR1-5	Diode, 1N4151	100385
CR6	Diode, 19330	019330
L1	Inductor, R45-4	101313
Q1	Transistor, MPF-152	101383
Q2	Transistor, 2N3906	101378
Q3,4	Transistor, 2N3904	101377
Q5,7	Transistor, MPF-105	101384
Q6	Transistor, 2N3565	101371
R2	Resistor, 100 Ω 5%, 1/4 W, CC	101609
R5,8,9,13,14, 19,28,51	Resistor, 10 k 5%, 1/4 W, CC	101570
R6,7,11,12	Resistor, 3.9 k 5%, 1/4 W, CC	101601
R10	Resistor, 1 k 5%, 1/4 W, CC	101569
R15,18	Resistor, 8.2 k 5%, 1/4 W, CC	101595
R16	Resistor, 5 k 62 PA, Var.	101845
R17	Resistor, 1 M 5%, 1/4 W, CC	101605
R20	Resistor, 100 k 62 PA, Var.	101934
R21	Resistor, 750 Ω 5%, 1/4 W, CC	101689
R22	Resistor, 6.8 k 5%, 1/4 W, CC	101544

PARTS LIST

SHAPER & MODULATOR #021556-7-5 (Cont'd)

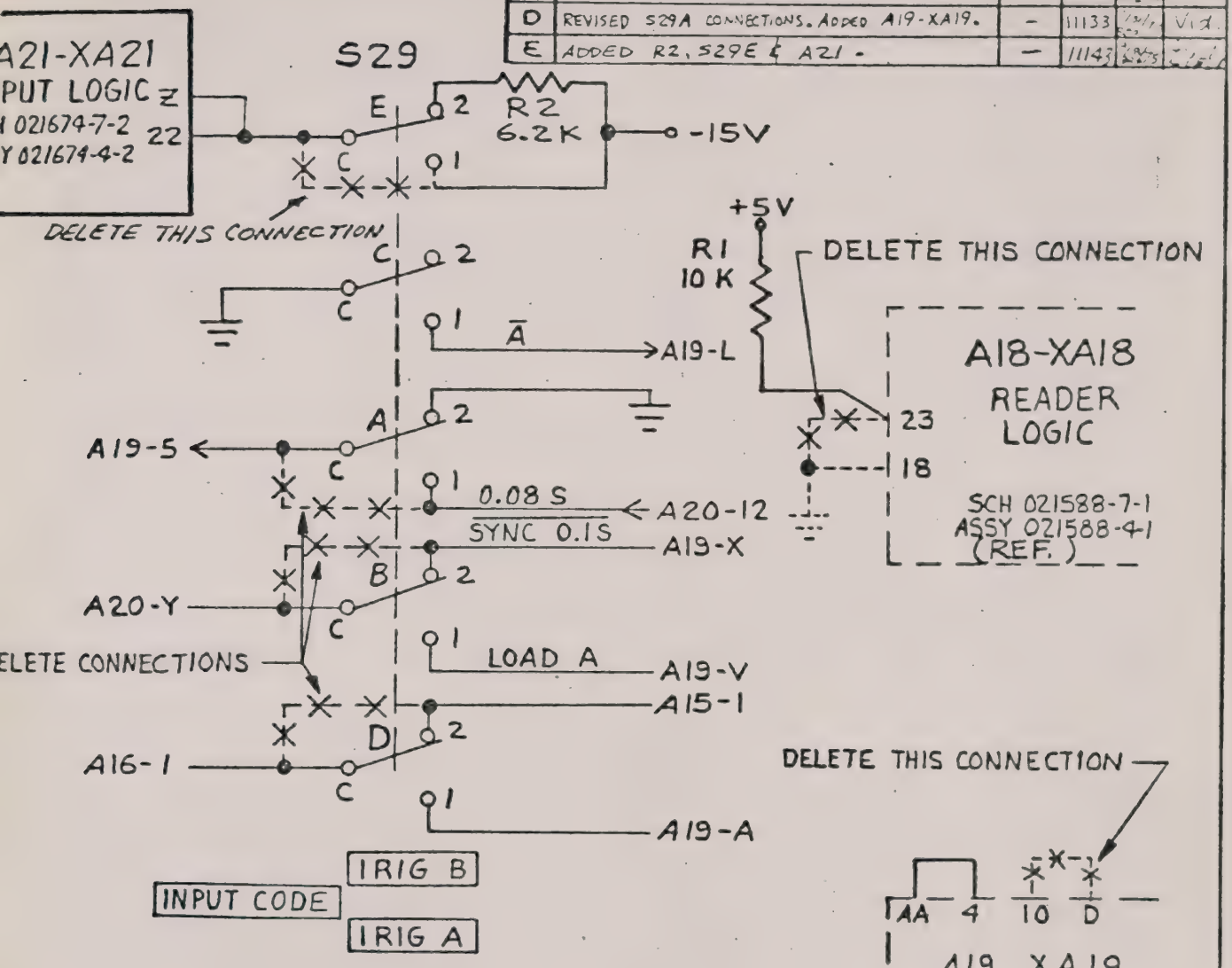
REF.	DESCRIPTION	SD PART NO.
R23	Resistor, 10 k 62 PA, Var.	101937
R24	Resistor, 18 Ω 5%, 1/4 W, CC	101727
R25	Resistor, 120 Ω 5%, 1/4 W, CC	101717
R26	Resistor, 560 Ω 5%, 1/4 W, CC	101583
R27	Resistor, 2.7 k 5%, 1/4 W, CC	101599
R49	Resistor, 68 k 5%, 1/4 W, CC	101597
R50	Resistor, 56 k 5%, 1/4 W, CC	101670
R52	Resistor, 5.6 k 5%, 1/4 W, CC	101584
R53	Resistor, 1 k 79 P, Beckman, Var.	101181
R55	Resistor, 47 k 5%, 1/4 W, CC	101574
R56	Resistor, 560 k 5%, 1/4 W, CC	101687
R57	Resistor, 220 k 5%, 1/4 W, CC	101610
	Extractor	100867

OPTION C41
SWITCH SELECTABLE IRIG A/B
SCHEMATIC #7-06163701

This option provides for reading of the IRIG A or B time code on a switch selectable basis in the Model 8155.

The switch S29, A, B, C (Dwg. #06163701) provides necessary logic levels for the reading of IRIG B when in 1 position or for the reading of IRIG A when in 2 position.

REVISIONS					
LTR	DESCRIPTION	ENG NO	ECO NO	DATE	APP'D
A	RELEASED TO RECORD				
B	ADDED WIRE DELETION.	—	-		
C	ADDED R1(10K) & S29D.	—	11040		
D	REVISED S29A CONNECTIONS. ADDED A19-XA19.	—	11133		
E	ADDED R2, S29E & A21.	—	11143		



NOTES

1. ADD S29 TO FRONT PANEL.
2. CHANGE A21, INPUT LOGIC CARD, FROM 021674-4-1 TO 021674-4-2.

PROPRIETARY DATA
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		DRAWN 9-11-74 DATE	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES DECIMAL TOLERANCE .X ±.03 .XX ±.01 ANGLES ±	SYNTRON DONNER CORPORATION CONCORD, CALIFORNIA	C41 OPTION IRIG A/B SWITCH SELECTABLE
		CHECK		CODE IDENT. 53347	
		ENGR DATE		MATERIAL	REV 7
3155 S/N 1000+		PROJ ENGR DATE			DWG NO 06163701 ISSUE E
USED ON	NEXT ASSY	Q.A. DATE			
APPLICATION		SCALE	DO NOT SCALE DRAWING	DWG SIZE A SH 1 OF 1	

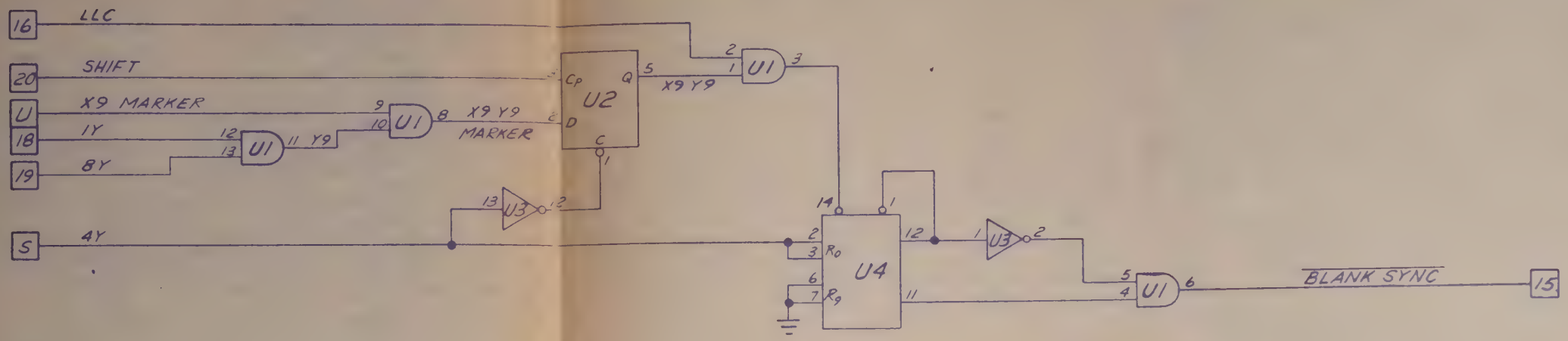
PARTS LIST

OPTION C41 IRIG A/B #7-06163701

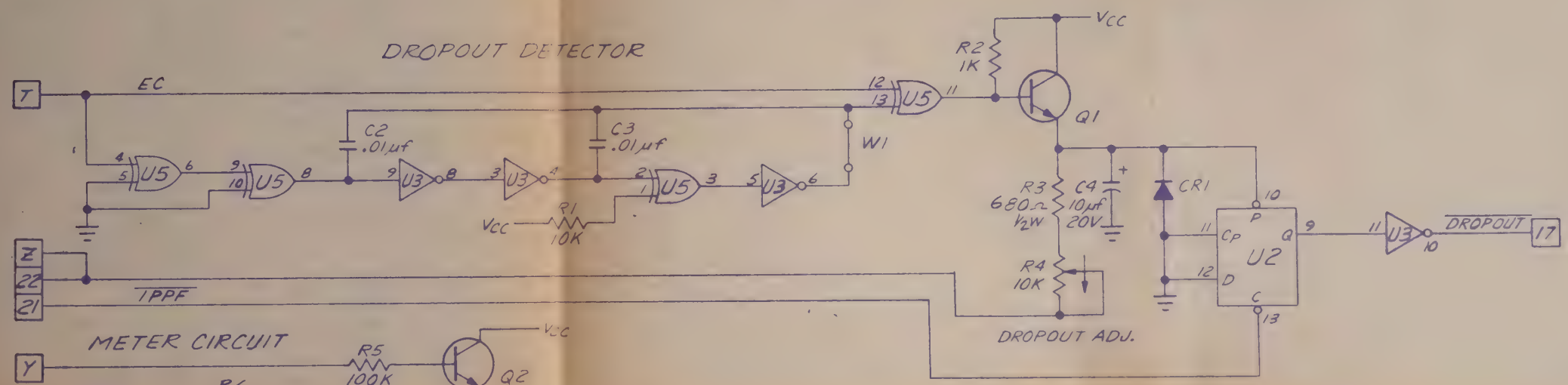
REF.	DESCRIPTION	SD PART NO.
	ADD	
	Schematic	7-06163701
A21	Assembly, Input Logic	021674-4-2
R1	Resistor, 10 k 5%, 1/4 W	101570
R2	Resistor, 6.2 k 5%, 1/4 W	101608
S20	Assembly, Rotary Switch	06134423
	DELETE	
A21	Assembly, Input Logic	021674-4-1
	Panel, Nomenclature	05115702

REVISIONS					
ISSUE	DESCRIPTION	SBR. NO.	ECO NO	DATE	APP BY
A	RELEASED TO RECORDS.	—	11143	4/9/75	G. M.

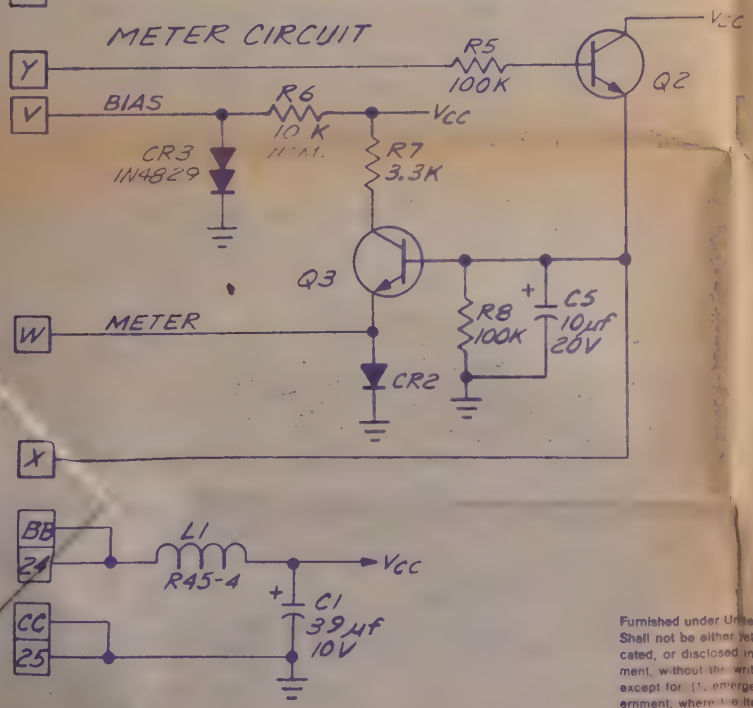
FRAME MARKER LENGTH DETECTOR



DROPOUT DETECTOR



METER CIRCUIT



NOTES: (UNLESS OTHERWISE SPECIFIED)

1. ALL DIODES ARE IN4151.
2. ALL RESISTORS ARE IN OHMS, ¼W, 5%.
3. ALL TRANSISTORS ARE 2N3904.
4. U4, PIN 5 TO V_{CC}, PIN 10 TO GND; ALL OTHER I.C.'S PIN 7 TO GND, PIN 14 TO V_{CC}.
5. U1 —— MC1806P
   U2 —— SN7474N
   U3 —— MC836P
   U4 —— SN7490N
   U5 —— MC1812P

ITEM NO	QTY	PART NUMBER	DESCRIPTION	SCHEMATIC REF. NO.

LIST OF MATERIALS

PROPRIETARY DATA

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		DRAWN 4-04-75 DATE	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES DECIMAL TOLERANCE X .XX .XXX ANGLES ±	SYSTRON DONNER CORPORATION CONCORD, CALIFORNIA	SCHEMATIC INPUT LOGIC
		CHECK DATE			
		ELECT. DATE			
		MECH. DATE			
		PROJECT 4/75 DATE		CODE IDENT. 53947	
8155A		APPROVAL DATE		MATERIAL	DWG NO. 21674-7-2 ISSUE A
USED ON	NEXT ASSY	SCALE	DO NOT SCALE DRAWING	DWG SIZE C	SH 1 OF 1
APPLICATION					

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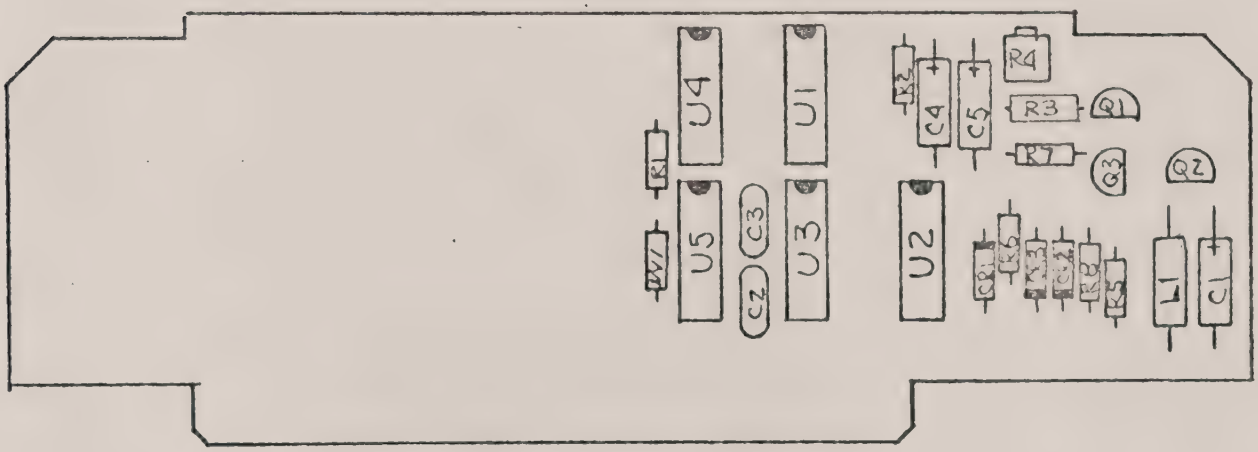
REVISIONS					
LTR	DESCRIPTION	ENG. APP.	DATE	APP'D	
A	RELEASED TO RECORDS.		11/17		



			SYSTRON DONNER CORPORATION CONCORD CALIFORNIA	ASS'Y., INPUT LOGIC PC BD,
8155			CODE IDENT 52947	
APPLICATION	1:1	SIZE C SHEET 1 OF 1		21674-9-1

PARTS LIST

INPUT LOGIC ASSEMBLY #021674-4-2

REF.	DESCRIPTION	SD PART NO.
	Assembly	021674-4-2
	Schematic	021674-4-2
C1	Capacitor, 39 µF, 10 V	100183
C2,3	Capacitor, .01 µF, 50 V	100105
C4,5	Capacitor, 10 µF, 20 V	100063
CR1,2	Diode, 1N4151	100385
CR3	Diode, 1N4829	100443
L1	Inductor, R45-4	101313
Q1-3	Transistor, 2N3904	101377
R1,6	Resistor, 10 k 5%, 1/4 W	101570
R2	Resistor, 1 k 5%, 1/4 W	101569
R3	Resistor, 680 Ω 5%, 1/2 W	101475
R4	Potentiometer, 10 k	101937
R5,8	Resistor, 100 k 5%, 1/4 W	101558
R7	Resistor, 3.3 k 5%, 1/4 W	101559
U1	Integrated Circuit, MC1806P	025733
U2	Integrated Circuit, SN7474N	025241
U3	Integrated Circuit, MC836P	025704
U4	Integrated Circuit, SN7490N	025732
U5	Integrated Circuit, MC1812P	025736

CIRCUIT DESCRIPTION
BCD MILLISECONDS (OPTION E14)
BASIC BLOCK DIAGRAM

1) GENERAL

The BCD Milliseconds Options, shown on the instrument Block Diagram, adds 14-pin rear panel connector J2 and associated wiring to the basic unit.

Parallel BCD Milliseconds outputs are supplied to J6 through buffers on Minor Counter Card (A20), see Chapter 5. These 12 bits have the following specifications:

Code:	8-4-2-1.
Logic:	"1" = +5 ±0.5 V behind 6 kΩ.
	"0" = 0 +0.5 V, 12 mA sink.

All outputs are short-circuit-proof to ground.

ITEM NO	PART NUMBER	DESCRIPTION	REFERENCE NUMBER	ASSY QTY
		DELETE FROM M8155A:		
1	021398111	COVER PLATE, 14 PIN CONN.	J2	1
		ADD THE FOLLOWING:		
1	101180	CONNECTOR, 14 PIN	J2	1
2		SCHEMATIC	D51206-7-1	REF
4	10062504	SCREW 2-56 x .2504		2
5	100661	WASHER #2 SPLIT		2
6	100636	NUT 2-56		2
7	100759	SOLDER LUG #2		1
9	101181	CONNECTOR, MATING 14 PIN	P2	1

A1 ITEM 2: SCH. 1/6 W495 TDC:120601 AT MFG 7-11-76

PREP R 5/13	EVERTON DONNER
CHECK	CODE IDENT. 06811
APPR.	MILLISECONDS E14 OPTION
8155A	P/L 051904-01 ISS A1
USED ON	SHEET 1 OF 1

CIRCUIT DESCRIPTION
DAYS (OPTION E20)
BASIC BLOCK DIAGRAM

1) GENERAL

The Days Option, shown on the instrument Block Diagram, adds Dwg. #21632-7-5 Days Accumulator (A8), #21657-7-1 Days Error Detector (A7), Leap Year switch S12, a colon and three-digit display to the Display Assembly (A102) and associated wiring to the basic unit.

Parallel BCD Days outputs are supplied to connector J1 through buffers on the Days Accumulator Card. These 12 bits (10 active) have the following specifications:

Code:	8-4-2-1.
Logic:	"1" = +5 ±0.5 V behind 6 kΩ.
	"0" = 0 +0.5 V, 12 mA sink.

All outputs are short-circuit-proof to ground.

PARTS LIST

OPTION E20 DAYS #05190501

REF.	DESCRIPTION	SD PART NO.
	ADD	
	Schematic	051206-7-1
A7	Assembly, Days Error Detector	021657-4-1
A8	Assembly, Accumulator	021632-4-5
C4	Capacitor, 1000 pF, DM15	100243
CR6,7	Lamp, LED	100455
S12	Switch, Slide	102630
U7-9	Integrated Circuit, DD700	045203
V4	Display, 3-Digit	102404
XA7,8	Connector, Edge	101204
	DELETE	
S12	Switch, Cover Plate	05120801

CIRCUIT DESCRIPTION
DAYS ERROR DETECTOR
SCHEMATIC #21657-7-1

1) GENERAL

The Days Error Detector card contains a three-decade accumulator which is updated on time, a parallel storage register for storing days bytes stripped from the input reference time code; a parallel comparator for comparing their contents and a days recycle circuit.

2) DAYS ACCUMULATOR

Each of the three-decade dividers (U8, U5 and U2) has data inputs which are connected to the storage register as the source of preset information. Grounding the preset input (pin C) loads the storage register contents into the accumulator. Each divider also has parallel outputs which are externally wired to the main Days Accumulator card. These lines along with the storage register outputs are connected to the parallel comparator.

3) STORAGE REGISTER

The Storage Register consists of quad latch chips U10, U7 and U4. These are loaded in two bytes, one representing units and tens of days and the other representing hundreds of days. This information is loaded as it is stripped from the reference input code. The first byte is strobed through inverters on U13 and the second is strobed through U1-8.

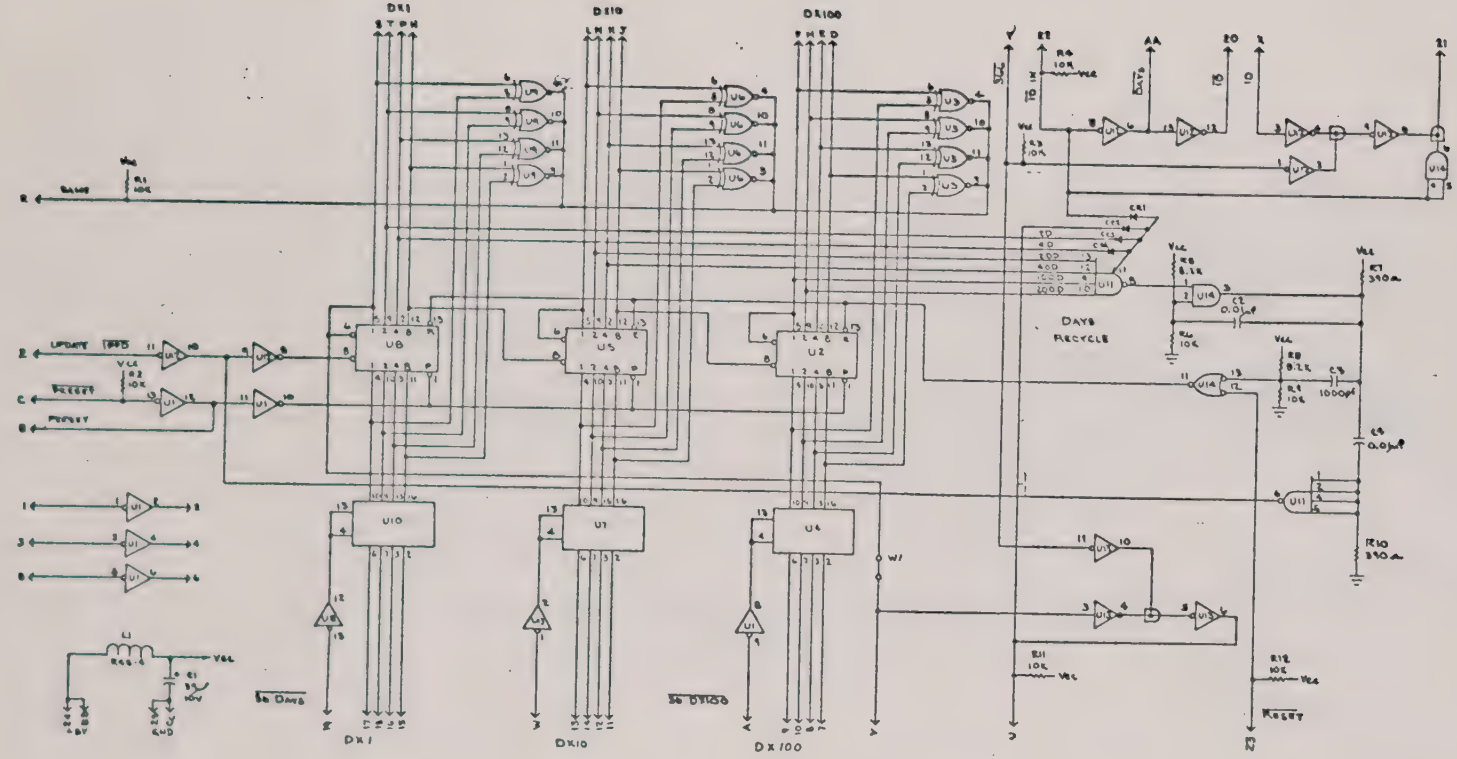
4) COMPARATOR

The parallel comparator is formed from gates on U9, U6 and U3. The output from each gate is tied to a common coincidence bus connected to pin R. This line goes positive when all bits in the accumulator match the coresponding bits in the Storage Register.

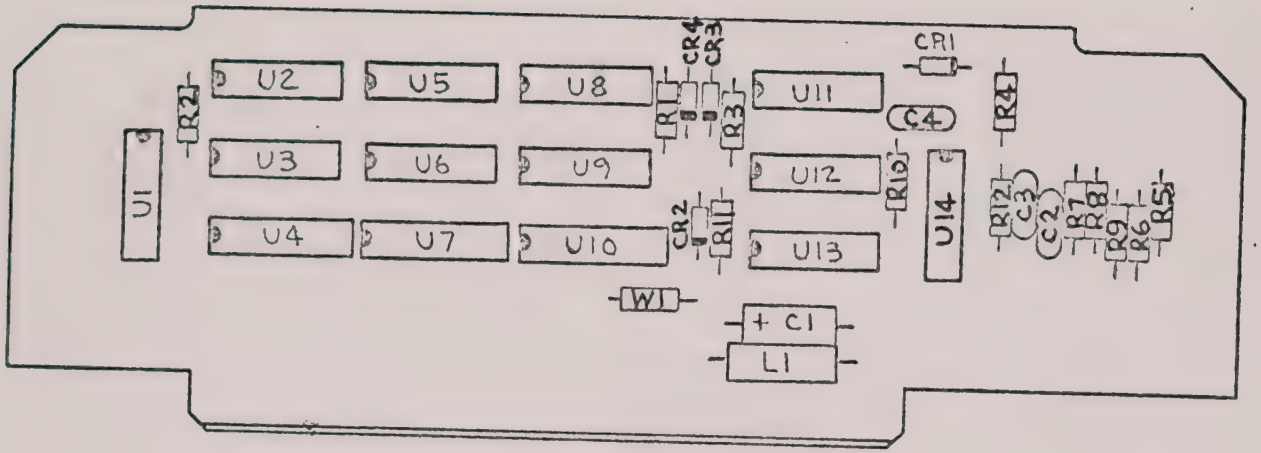
Operation is as follows: A strobe signal developed on the Control Logic card samples the comparator output during Y9 time after the Reader data has been loaded into the Storage Register. On the trailing edge of this strobe these data are transferred into the Accumulator by the preset input. (if the system in is sync with the reference code, the Accumulator will already contain this same information.) The coincidence output at pin R is connected to the TOD bus on the TOD Error Detector card and to the tenths-of-seconds bus on the Control Logic card. When all bits from .1s through days are in agreement, this bus goes positive, indicating a "good" frame. (See Control Logic card description.) The contents of the Accumulator are transferred to the main Accumulator when the selected number (usually three) of "good" frames are counted.

5) DAYS RECYCLE

The Days Recycle circuit detects 366 or 367 days (selected by leap year switch) and presets the Accumulator to 001. NAND gate U11-8 decodes the selected number of days and fires one-shot U14-3,11. The output from U14-11 resets the Accumulator to 000. The differentiated trailing edge of the resulting pulse from U14-3 through U11-6 and U12-8 loads in the "1". Provision is also made to inhibit recycle so that reset is to 000 at a count of 1000.



DAYS ERROR DETECTOR SCHEMATIC #21657-7-1 REV A



DAYS ERROR DETECTOR ASSEMBLY #21657-4-1

PARTS LIST

DAYS ERROR DETECTOR #021657-7-1 REV A_n

REF.	DESCRIPTION	SD PART NO.
	Assembly	021657-4-1
	Schematic	021657-7-1
C1	Capacitor, 39 µF, 10 V, 150 D-B	100183
C2,4	Capacitor, .01 µF, Disc.	100103
C3	Capacitor, 1000 pF, DM15	100243
CR1-4	Diode, 1N4151	100385
L1	Inductor, R45-4	100313
R1-4,6,9,11,12	Resistor, 10 k 5%, ¼ W	100570
R5,8	Resistor, 8.2 k 5%, ¼ W	101595
R7,10	Resistor, 390 Ω 5%, ¼ W	101592
U1,12,13	Integrated Circuit, MC836P	025704
U2,5,8	Integrated Circuit, N8280A	025722
U3,6,9	Integrated Circuit, N8242A	025755
U4,7,10	Integrated Circuit, SN7475N	019710
U11	Integrated Circuit, MC830P	019712
U14	Integrated Circuit, MC1806P	025733
W1	Jumper, Molded	102879
	Extractor	100865

CIRCUIT DESCRIPTION
DAYS ACCUMULATOR
SCHEMATIC #21632-7-5

1) GENERAL

The Days Accumulator card can provide up to three serial decades with common reset, parallel preset and two sets of buffered, parallel BCD outputs. Provision is made to gate one set of BCD outputs in three 4-bit bytes. The input may be either ac or dc-coupled and fed to the first decade through an update inhibit circuit. A days recycle circuit is included which may be programmed to reset the accumulator to 001 at the end of 365 or 366 days.

2) DECADE DIVIDERS

The up to three decade dividers are connected in tandum. Each is provided with parallel BCD data inputs which may be used to load preset information when the associated data strobe ($\overline{\text{PRESET}}$) line is grounded. Jumpers W1 and W2 permit the data strobe associated with the center decade (A4) to be wired in common with the data strobe input to the first decade (A1) or the third (A6). The decade zero-reset inputs are wired in common through buffers on A8 to pin 23. The parallel BCD outputs from each decade are wired to output pins through two sets of buffers.

3) OUTPUT BUFFERS

The BCD output buffers may be inverting or noninverting. One of the two sets (A10,A13 and A15) can be gated by inputs through pins L, K and J, respectively. These gate lines are buffered by inverters A11.

4) INPUT INHIBIT CIRCUIT

This circuit allows the presence of a ground on pin H to inhibit input signals on pin F from updating the accumulator. Gate A2-6 inverts and buffers the input. Gates A2-11 and A2-8 form an RS flip-flop.

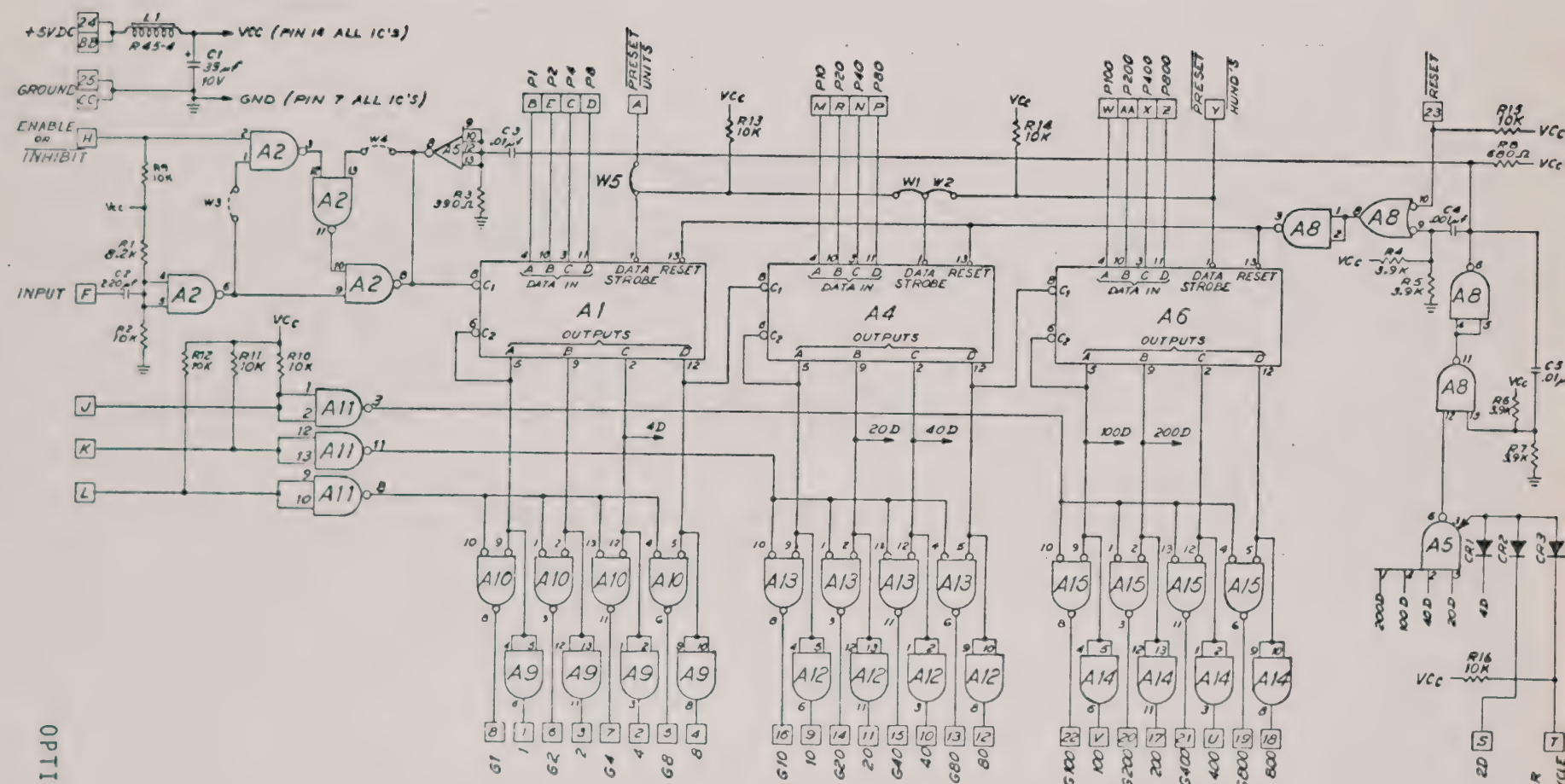
A2-3 gates the $\overline{\text{INHIBIT}}$ line and the inverted input. When the accumulator is updating, flip-flop A2-8,11 output follows the input. When the $\overline{\text{INHIBIT}}$ line, pin H, is grounded,the flip-flop will latch with the output high. The output will go low the first time the input is low after the ground has been removed from the $\overline{\text{INHIBIT}}$ line.

5) DAYS RECYCLE CIRCUIT

Gate 5-6 is a four-input NAND gate with an expander input. The connection of diodes CR1-CR3 gives the gate seven inputs. If recycle at 366 is desired, pin T is connected to Vcc. If recycle at 367 (for leap

year) is desired, pin T is connected to pin 1 (the one day output). Pin S is always connected to the two day output. At the selected count, the output of A5-6 will go low, triggering one-shot A8-11,6. The one-shot output is a negative-going pulse (from +5 to 0 V). The leading edge of the pulse (ac-coupled into A8-8) causes the three dividers to reset to 000. The trailing edge of the pulse (which is positive-going) is ac-coupled into A5-8 where it is inverted and used to input one count to the first decade. The resulting accumulator contents are 001.

21632-7-5



DAYS ACCUMULATOR SCHEMATIC #21632-7-5 REV B

OPTION E13-4

DAYS ACCUMULATOR ASSEMBLY #21632-4-1 REV B

PARTS LIST

DAYS ACCUMULATOR #21632-7-5

REF.	DESCRIPTION	SD PART NO.
	Assembly (Ref. Assy. Dwg. #21632-4-1)	21632-4-5
	Schematic	21632-7-5
A1,4,6	Integrated Circuit, N8280P	25722
A2,11	Integrated Circuit, MC846P	19716
A5	Integrated Circuit, MC830P	19712
A8	Integrated Circuit, SN7400N	19705
A9,12,14	Integrated Circuit, MC1806P	25733
A10,13,15	Integrated Circuit, MC1808P	25734
C1	Capacitor, 39 µF, 10 V	C0902
C2	Capacitor, 220 pF	C0161
C3,5	Capacitor, .01 µF, Disc	C0556
C4	Capacitor, .001 µF, Disc	C0235
CR1-3	Diode, 1N4151	CR0150
L1	Inductor, R45-4	L0143
R1	Resistor, 8.2 k, 1/4 W, 5%	R0883
R2,9-16	Resistor, 10 k, 1/4 W, 5%	R0766
R3	Resistor, 390 Ω, 1/4 W, 5%	R0880
R4-7	Resistor, 3.9 k, 1/4 W, 5%	R0939
R8	Resistor, 680 Ω, 1/4 W, 5%	R1234
W1,2,5	Jumper, Molded	W0087
	Extractor	H1743

CHAPTER 7
SPECIAL MODIFICATIONS

7.1 GENERAL

Modifications to the Model 8155, requested by the customer, are documented in this chapter. These are usually extra-cost items to tailor the unit for a specific application.